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A REPORT ON THE EVALUATION

Electronic Numerical Integrator

Report of Work under Contract No. DA-36-074-ORD-4646

Between

Ordnance Department, United States Army
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and

The University of Pennsylvania
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PART II

TECHNICAL DESCRIPTION OF THE SERIES

by

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DESCRIPTION TO
GENERAL INFORMATION

0. INTRODUCTION

The ENIAC consists of the following parts, as follows:

- 1) Operating Manual
- 2) Maintenance Manual
- 3) Technical Description of the ENIAC
Volume I - Chapters I to VI
Volume II - Chapters VII to XII
- 4) Part I, Technical Description of the ENIAC
Volume II - Chapters VII to XII
- 5) Part II, Technical Description of the ENIAC

Included with the Operating Manual and Part I of the Technical Description are all drawings (see Table 0.3 below) which are necessary for understanding these reports. The Maintenance Manual assumes access to the file of all drawings.

Part I of the Technical Description is intended for those who are to have a general understanding of how the ENIAC works, and concerning themselves with the details of the circuits; it assumes no knowledge of electronics or circuit theory. Part II is intended for those who require a detailed understanding of the circuits. Its organization, from the start, duplicates that of Part I so as to make cross referencing between the two parts easy.

The ENIAC Operating Manual contains a complete set of instructions for operating the ENIAC. It includes very little explanatory material, and hence assumes familiarity with Part I of the Technical Description of the ENIAC. The ENIAC Maintenance Manual includes description of the various test units and procedures for testing, as well as a list of common and probable sources of trouble. It assumes a complete understanding of the details of the ENIAC, i.e., a knowledge of both Parts I and II of the Technical Description of the ENIAC.

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The Report on the ENIAC and the complete file of ENIAC drawings constitute a complete description and set of instructions for operation and maintenance of the machine. The drawings carry a number of the form PX-n-m. The following tables give the classification according to this numbering system.

TABLE O.1	
Values of n	Division
1	General
2	Test Equipment
3	Racks and Panels
4	Trays, Cables, Adaptors, and Load boxes
5	Accumulators
6	High Speed Multiplier
7	Function Table
8	Master Programmer
9	Cycling Unit and Initiating Unit
10	Divider and Square Root
11	Constant Transmitter
12	Printer
13	Power Supplies

TABLE O.2	
Values of m	Subject
101-200	Wiring Diagrams
201-300	Mechanical Drawings
301-400	Report Drawings
401-500	Illustration Problem Set-Ups

The reader of this report will be primarily interested in the types of drawings listed in the following paragraphs. A table on page 4 gives the corresponding drawing number for each unit of the ENIAC.

1) Front Panel Drawings. These drawings show in some detail the switches, sockets, etc., for each panel of each unit. They contain the essential instructions for setting up a problem on the ENIAC.

2) Front View Drawings. There is one of these drawings for each kind of panel used in the various units of the ENIAC. These show the relative position of the trays and the location of the various neon lights. Since these drawings show the neon lights, they can be used to check the proper operation of the various units.

3) Block Diagrams. These drawings illustrate the logical essentials of the internal circuits of each unit. That is, resistors, condensers, and some other electrical details are not shown; but complete channels (paths of pulses or gates representing numbers or program signals) are shown in all their multiplicity. These drawings will be of interest to those who are interested in Parts I and II of the Technical Report.

4) Cross-section Diagrams. These drawings are electronically complete except that only one channel is shown where there is more than one. Thus, these drawings show every resistor and condenser and any other electronic elements belonging to any circuit. These drawings will be of particular interest to the maintenance personnel and to those reading Part II of the technical report.

5) Detail Drawings. All other drawings of the ENIAC come under this heading. A complete file of drawings is available at the location of the ENIAC.

Part 0.3
 called by ATACS

Unit	Front Panel	Front View	Block Diagram	Cross - Section
Initiating Unit	PX-9-302 9-302R	PX-9-305	PX-9-307	
Cycling Unit	PX-9-303 9-303R	PX-9-304	PX-9-307	
Accumulator	PX-5-301	PX-5-305	PX-5-304	PX-5-115
Multiplier	PX-6-302 6-302R 6-303 6-303R 6-304 6-304R	PX-6-309	PX-6-308	PX-6-112A 6-112B
Function Table	PX-7-302 7-302R 7-303 7-303R	PX-7-305	PX-7-304	PX-7-111 7-118
Divider and Square Root	PX-10-301 10-301R	PX-10-302	PX-10-304	
Constant Transmitter	PX-11-302 11-302R 11-303 11-303R 11-304 11-304R	PX-11-306	PX-11-307	PX-11-116 11-309 (C.T. and R.)
Printer	PX-12-301 12-301R 12-302 12-302R 12-303 12-303R	PX-12-306	PX-12-307	PX-12-115
Master Programmer	PX-8-301 8-301R 8-302 8-302R	PX-8-305	PX-8-304	PX-8-104

Other drawings of particular interest:

Floor Plan	PX-1-302	IBM Punch and Plugboard	PX-12-112 PX-12-305
A.C. Wiring	PX-1-303	Pulse Amplifier and Block Diagram	PX-4-302 PX-4-301
IBM Reader and plugboard	PX-11-119 PX-11-305	Interconnection of Multiplier and Accumulators	PX-6-311
		Interconnection of Divider and Accumulators	PX-10-307

The front view drawings and the large front panel drawings (whose numbers do not end with "R") are bound as a part of the Operator's Manual.

Included with the report is a folder containing all the drawings listed in the above table except the large front panel (see above). A complete file of drawings is available at the location of the ENIAC.

TABLE OF CONTENTS

I. GENERAL DESCRIPTION OF THE ENIAC

1.1. BRIEF DESCRIPTION OF THE ENIAC	Page 2
1.1.1. <u>Units of the ENIAC</u>	3
1.1.2. <u>Digit Trunks</u>	7
1.1.3. <u>Program Trunks</u>	8
1.1.4. <u>Static Cables</u>	8
1.2. FUNDAMENTAL ELECTRONIC UNITS OF THE ENIAC	8
1.2.1. <u>Flip-flop</u>	9
1.2.2. <u>Counters</u>	11
1.2.3. <u>Gate Tubes</u>	13
1.2.4. <u>Buffer Tubes</u>	15
1.2.5. <u>Cathode Followers</u>	16
1.2.6. <u>Inverter Tubes</u>	16
1.2.7. <u>Pulse Standardizer</u>	17
1.2.8. <u>Transmitter</u>	19
1.2.9. <u>Receiver Plug-in Unit</u>	20
1.2.10. <u>Transceiver Plug-in Unit</u>	21
1.3. BLOCK AND CROSS SECTION DIAGRAMS	22

II. INITIATING UNIT

2.1. STARTING AND STOPPING SEQUENCE AND INITIAL CLEAR	2
2.1.1. <u>Normal Initial Conditions</u>	2
2.1.2. <u>Complete Starting Sequence</u>	4

2.1.3. <u>The d-c ~~off~~ Sequence</u>	Page 6
2.1.4. <u>The d-c on Sequence</u>	7
2.1.5. <u>The Initial Clear</u>	8
2.2. INITIATING PULSE PROGRAM CONTROL	11
2.3. OTHER FEATURES	12
2.3.1. <u>Selective Clear Controls</u>	12
2.3.2. <u>Reader and Printer Program Controls</u>	13
2.4. TESTING FEATURES	

III. CYCLING UNIT

3.0. INTRODUCTION	2
3.1. THE OSCILLATOR AND PULSE FORMERS	3
3.1.1. <u>The Oscillator</u>	3
3.1.3. <u>The on-beat plug-in unit</u>	4
3.1.4. <u>The off-beat plug-in unit</u>	5
3.2. THE RING AND ITS ASSOCIATED GATES AND FLAP-FLOPS	5
3.2.1. <u>The tens pulses (10P)</u>	5
3.2.2. <u>The 1, 2, 2', 4 and 9 pulses</u>	6
3.2.3. <u>The one-primed pulse (1'P)</u>	7
3.2.4. <u>The carry clear gate (CCG)</u>	7
3.2.5. <u>The reset pulse (RP)</u>	8
3.2.6. <u>The central program pulse (CPD)</u>	8

3.3. ONE PULSE AND ONE ADDITION TIME OPERATION	8
3.3.1. <u>One addition time operation</u>	9
3.3.2. <u>One pulse time operation</u>	9

IV. ACCUMULATOR

4.0. INTRODUCTION	2
4.1. THE PROGRAM CONTROL CIRCUITS	5
4.1.1. <u>General description of a non-repeat program control circuit</u>	5
4.1.2. <u>General description of a repeat program circuit</u>	6
4.2. THE COMMON PROGRAMMING CIRCUITS	7
4.2.1. <u>The receiving circuits</u>	7
4.2.2. <u>The add and subtract transmission circuits</u>	8
4.2.3. <u>General description of the clear circuits</u>	9
4.2.4. <u>A description of the interconnection features</u>	10
4.3. NUMERICAL CIRCUITS	
4.3.1. <u>General description of decade plug-in unit</u>	11
4.3.2. <u>General description of a PM - Clear plug-in unit</u>	15

V. THE HIGH SPEED MULTIPLIER

5.0. INTRODUCTION	2
5.1. PROGRAM CONTROL CIRCUITS	3
5.1.1. <u>The buffer plug-in units</u>	3
5.1.2. <u>Transceivers</u>	4
5.1.3. <u>Program control switches</u>	4

5.2. COMMON PROGRAMMING CIRCUITS	Page 6
5.2.1. <u>The multiplier ring</u>	6
5.3. INITIAL CLEARING	9
5.4. NUMERICAL CIRCUITS	10
5.4.1. <u>The multiplier selector</u>	10
5.4.2. <u>The tables and the table gates</u>	10
5.4.3. <u>The multiplicand selectors</u>	11
5.5. EXAMPLE	13

VI. DIVIDER AND SQUARE-ROOTER

6.0. INTRODUCTION	2
6.1. PROGRAM CONTROLS	3
6.1.1. <u>Numerator and denominator receive switches</u>	3
6.1.2. <u>The numerator and denominator clear switches</u>	4
6.1.3. <u>Interlock Switch</u>	5
6.1.4. <u>Answer disposal switch</u>	5
6.1.5. <u>Round-off Switch</u>	6
6.1.6. <u>Root-Divide and Place Switch</u>	6
6.2. THE COMMON PROGRAMMING CIRCUITS	7
6.2.1. <u>The pulse source circuits</u>	8
6.2.2. <u>The program ring circuits</u>	10
6.2.3. <u>The Sign Indication Circuit</u>	12
6.2.4. <u>The over-draft circuit</u>	14
6.2.5. <u>The add-subtract circuit</u>	15

5.2. COMMON PROGRAMMING CIRCUITS	Page 6
5.2.1. <u>The multiplier ring</u>	6
5.3. INITIAL CLEARING	9
5.4. NUMERICAL CIRCUITS	10
5.4.1. <u>The multiplier selector</u>	10
5.4.2. <u>The tables and the table gates</u>	10
5.4.3. <u>The multiplicand selectors</u>	11
5.5. EXAMPLE	13

VI. DIVIDER AND SQUARE-ROOTER

6.0. INTRODUCTION	2
6.1. PROGRAM CONTROLS	3
6.1.1. <u>Numerator and denominator receive switches</u>	3
6.1.2. <u>The numerator and denominator clear switches</u>	4
6.1.3. <u>Interlock Switch</u>	5
6.1.4. <u>Answer disposal switch</u>	5
6.1.5. <u>Round-off Switch</u>	6
6.1.6. <u>Root-Divide and Place Switch</u>	6
6.2. THE COMMON PROGRAMMING CIRCUITS	7
6.2.1. <u>The pulse source circuits</u>	8
6.2.2. <u>The program ring circuits</u>	10
6.2.3. <u>The Sign Indication Circuit</u>	12
6.2.4. <u>The over-draft circuit</u>	14
6.2.5. <u>The add-subtract circuit</u>	15

6.2.6. <u>The round-off circuit</u>	Page 17
6.2.7. <u>The root correction circuit</u>	18
6.2.8. <u>The shift circuit</u>	19
6.2.9. <u>The interlock and clear circuits</u>	20
6.2.10. <u>The initial clear</u>	21
6.3. NUMERICAL CIRCUITS	21
6.3.1. <u>The quotient-place ring</u>	21
6.4. EXAMPLES	24
6.4.1. <u>A division example</u>	24
6.4.2. <u>A square root example</u>	28

VII. FUNCTION TABLE

7.0. INTRODUCTION	2
7.1. THE PROGRAM CONTROL CIRCUITS	3
7.1.1. <u>The Transceivers</u>	3
7.1.2. <u>The Argument Reception Switch</u>	3
7.1.3. <u>The Program Switch</u>	4
7.1.4. <u>The Repeat Switch</u>	6
7.2. THE COMBINATION PROGRAMMING CIRCUITS	6
7.2.1. <u>The Program Ring</u>	6
7.2.2. <u>The Argument Flip-flop</u>	8
7.2.3. <u>The Add and Subtract Flip-flops and the Pulse Gates</u>	8
7.2.4. <u>Use of the Function Table for Programming</u>	9
7.2.5. <u>Initial Clear</u>	10

7.3. THE NUMERICAL CIRCUITS	Page 10
7.3.1. <u>The Argument Rings</u>	10
7.3.2. <u>The Table Input Gates</u>	12
7.3.3. <u>The Portable Table</u>	13
7.3.4. <u>Table Output Gates</u>	13
7.3.5. <u>The PM Master Switches</u>	14
7.3.6. <u>The constant switches and the delete switches</u>	14
7.3.7. <u>The Subtract Pulse Switches</u>	15
7.3.8. <u>The output transmitters</u>	15
7.3.9. <u>adapters</u>	16

VIII. THE CONSTANT TRANSMITTER AND IBM READER

8.1. CONSTANT TRANSMITTER PROGRAM CONTROLS	2
8.1.1. <u>The groups of numbers</u>	2
8.1.2. <u>Transceivers</u>	3
8.1.3. <u>The Program Control Circuits</u>	3
8.2. READER PROGRAM CONTROLS	6
8.2.1. <u>Starting</u>	6
8.2.2. <u>Resetting</u>	6
8.2.3. <u>The Finish Signal</u>	7
8.2.4. <u>Interlock</u>	7
8.3. NUMERICAL CIRCUITS OF THE CONSTANT TRANSMITTER	8
8.3.1. <u>The Storage Relays and their Gates</u>	9
8.3.2. <u>The Constant and PM Set Switches</u>	11

8.4. THE IBM READER	Page 13
8.4.1. <u>The a-c Circuits</u>	13
8.4.2. <u>Starting Circuits</u>	13
8.4.3. <u>Numerical Circuits</u>	15
8.4.4. <u>Group Selection</u>	16
8.4.5. <u>Reset Control and Reset Shunt</u>	16
8.4.6. <u>Coding Cams</u>	17
8.4.7. <u>Reset Signal</u>	18
8.4.8. <u>Finish Signal</u>	18

IX. PRINTER AND IBM GANG PUNCH

9.1. PROGRAM CONTROL CIRCUITS	3
9.1.1. <u>The Printing Switches</u>	3
9.1.2. <u>Starting Circuit</u>	3
9.1.3. <u>Reset and Program Output</u>	3
9.1.4. <u>The Interlock Cam</u>	5
9.1.5. <u>Initial Clear</u>	6
9.2. THE NUMERICAL CIRCUITS OF THE PRINTER	6
9.3. THE IBM GANG PUNCH	10
9.3.1. <u>The a-c Circuit</u>	10
9.3.2. <u>The Starting Circuit</u>	11
9.3.3. <u>The Column Splits (PM Circuits)</u>	12
9.3.4. <u>The Punch Magnets</u>	12
9.3.5. <u>The Emitter</u>	13
9.3.6. <u>The Plug-board</u>	13

X. MASTER PROGRAMMER

10.1. INTRODUCTION	Page 1
10.2. DECADE COUNTER CIRCUITS	1
10.2.1. <u>Decade ring</u>	1
10.3. THE STEPPER CIRCUITS	4
10.3.1. <u>The stepper ring</u>	4
10.3.2. <u>The program transmitters</u>	6
10.3.3. <u>The program receiving circuit</u>	7
10.3.4. <u>The coincidence gates</u>	7
10.4. ASSOCIATION SWITCHING	9

XI. THE TRANSMISSION SYSTEM AND SPECIAL DEVICES

11.1. TRAYS AND TRUNKS	1
11.1.1. <u>Trays</u>	1
11.1.2. <u>Jumpers</u>	2
11.1.3. <u>Trunks and Lines</u>	2
11.1.4. <u>Load Boxes</u>	3
11.1.5. <u>Load Units</u>	3
11.2. DELETTERS	5
11.3. SHIFTERS	5
11.4. PULSE AMPLIFIER UNIT	6
11.5. STATIC OUTPUTS	7

11.6. SPECIAL DEVICES

Page 8

11.6.1. <u>Special Program Jumpers</u>	8
11.6.2. <u>Accumulator Interconnection Cables</u>	8
11.6.3. <u>Multiplier Interconnection Cables</u>	8
11.6.4. <u>Divider Interconnection Cables and Adapters</u>	9
11.6.5. <u>Function Table Adapters</u>	9
11.6.6. <u>Other Adapters</u>	10

TECHNICAL DESCRIPTION OF THE ENIAC, PART II.

This part of the report describes in some detail the circuits used in the various units of the ENIAC. Only sufficient programming details, that is, switch settings and plugging details, will be given to enable the reader to understand the circuits. For more detailed programming and illustrative set-ups the reader is referred to the corresponding chapters and sections of part I of this report.

I. GENERAL DESCRIPTION OF THE ENIAC

This chapter describes the arrangement of the units of the ENIAC, gives a summary of its mode of operation, and describes certain vacuum tube and circuit arrangements which are used repeatedly in the units of the ENIAC.

1.1. Brief description of the ENIAC.

The ENIAC is an extremely high speed electronic numerical computing device. It performs sequences of computations (without manual attention except for setting up) which are made up of the following operations,

1. Reading initial data from IBM cards
2. Addition
3. Subtraction
4. Multiplication
5. Division
6. Square-rooting
7. Looking up function values in function tables
8. Punching the results on IBM cards.

Generally, the units of the ENIAC have been designed to carry on the above operations using ten digit decimal numbers. In case greater accuracy is desired provision has been made to carry on the above operations using twenty digit decimal numbers. Actually there is an upper limit to the number of different steps of computation that can be performed without the attention of the operator, but this upper limit has been made high enough to handle a very large class of computing problems.

The ENIAC is a discrete variable rather than a continuous variable device. Consequently, errors in computation arise only from mathematical considerations (such as truncation, that is, the replacing of derivatives by difference quotients, and rounding-off errors) or from failure of some circuit in the device. Careful attention was given to minimizing failures and for

easy location and repair of them when they occur. The ENIAC uses the decimal system, and handles negative numbers by means of complements with respect to 10^n .

1.1.1. Units of the ENIAC

Table 1-1 gives a list of the units of the ENIAC, the number of program controls of each, and the purpose of each unit. Essentially, the number of program controls determines how many times that unit may be used for a different purpose in a particular sequence of computations.

(The Initiating Unit. Besides a hum oscilloscope to check the a-c supply lines and voltmeters to read the various a-c and d-c voltages, the initiating unit has the following switch controls:

- 1) Start Switch - Turns on the cooling fans and the heaters. The amber light indicates that the switch has been thrown.
- 2) D-C On-Off Switch.- This switch is located on the fuse panels. It can be used to turn the d-c power on and off.
- 3) Stop Switch - Turns off all the power.
- 4) Initial Clear - Clears all the units in preparation for starting a sequence of computations. Green light comes on when initial clear has occurred.
- 5) Door shunt switch - Enables the ENIAC to be operated for checking purposes with some of the back covers off.
- 6) Reader Start Switch - Causes the IBM Reader to read a card and then give out a program pulse which can be used for starting a sequence of computations. The Reader can be caused to operate by a program pulse as well as by use of this switch.
- 7) Initiating Pulse Switch - This switch causes a synchronized program pulse to be given out. This can be used to start a sequence of computations.

The initiating unit contains selective clear program controls by which certain predetermined accumulators can be caused to clear. The printer program controls are also located in the initiating unit. A clock which measures the time the power supply heaters are on is also located on this panel.

Cycling Unit. This unit produces the pulses which are used to represent digits or program signals, and causes the various units of the ENIAC .

TABLE 1-1

Units of the ENIAC

Number of units	Name of unit	Number of program controls per unit	Purpose
1	Initiating unit	6	Control center for starting and stopping computations. Contains six selective clear program controls.
1	Cycling unit	---	Pulse and gate producing unit which causes the other units of the ENIAC to operate in synchronism.
20	Accumulator	12	Each accumulator can store ten digit numbers, add numbers (transmitted by other units) to its contents, or transmit its number and/or its complement to other units and clear.
1	High-Speed Multiplier	24	This unit makes use of built-in multiplication tables to perform high-speed multiplication.
1	Divider-Square rooter	11	This unit divides two, ten or twenty digit numbers and extracts the square roots of ten or twenty digit numbers.
3	Function table	11	These units can look up the values of functions. The values of the functions must be set up on switch panels by the operator.
1	Constant Transmitter and IBM reader	3	This unit reads initial data from IBM cards, sets it up on relays and transmits it electronically. The IBM reader program control is located in the initiating unit.
1	Printer and IBM punch	1	This unit causes the results of sequences of computations to be punched on IBM cards. The IBM Gang punch program control is located in the initiating unit.
1	Master programmer	---	This is a program control device which decides when to change from one sequence of computations to another, or when to print and when to read more initial data.
Program trunks and digit trunks			These are transmission lines which make it possible to transfer numbers and program signals from unit to unit as needed.

to operate in synchronism. Table 1-2 lists the kinds of pulses and gates that are produced at this unit and transmitted to the other units over the cycling trunk.

Accumulator. Depending upon the switch settings, digit trunk connections, and program trunk connections an accumulator can accomplish the following things:

- 1) Store a ten digit number or its complement and a PM indication determining which it is.
- 2) Transmit over a digit trunk the number, its complement, or both, after transmitting it may or may not clear as desired.
- 3) Add to its contents a positive or negative number transmitted by some other unit of the ENLAC, properly indicating the sign of the sum.
- 4) All accumulators may transmit their contents by means of static cables to either the multiplier or the printer. Certain accumulators are semi-permanently connected to the printer. The sign indication is transmitted to the divider in this manner.

Multiplier. The multiplier multiplies a ten digit multiplicand by an n ($n \leq 10$) digit multiplier in $n+4$ addition times and rounds off the answer to any prescribed number of places if so desired. To do this, the multiplier makes use of four or six accumulators. This high-speed multiplication is accomplished by means of built-in multiplication tables.

Divider-Square Root. This unit can divide ten or twenty digit numbers and can extract the square root of a ten or twenty digit number. If p is the setting of the places switch a division takes $10 + 2$ (number of trial subtractions) + $2p$ addition times.

Function Table. The function table working in conjunction with either a variable or a permanent table can transmit any one of 104 values of a function (or if less than seven digits is needed 208 values of the function). To facilitate interpolation, arrangement has been made to transmit any one of the four neighboring values if desired. If a functional value is to be transmitted r times ($1 \leq r \leq 9$) the process of obtaining the functional value takes

TABLE 1-2

Kind of pulse or gate	Remarks
CPP Central Program Pulse	Used as a program pulse.
10P Tens Pulses	Used to cycle the decades of accumulators when transmitting a number over the add or subtract outputs.
9P Nines Pulses	Various combinations of these pulses are used to represent the digits 0, 1, ..., 9.
1P One Pulse	A coded system makes use of various combinations of these groups to represent the digits 0, 1, 2, ..., 9.
2P Two Pulses	
2'P Two-primed Pulses	
4 P Four Pulses	
1'P One-primed Pulse	Generally used as a correction pulse in taking complements (negative numbers).
COG Carry-Clear Gate	Used to take care of carry-over in the decades of the accumulators and to clear accumulators when so programmed.
RP Reset Pulses	These pulses are used to reset decade flip-flops in the accumulators and to provide the delayed carry-over pulse.

The time unit of operation for the ENLAC is one addition time. This is normally a time interval of 200 micro-seconds. An addition time is divided into 20 pulse times, each 10 micro-seconds long. The pulses listed in the above table arrive via the cycling trunk at each unit of the ENLAC once each addition time. The pulse times at which the various pulses and gates are produced is illustrated by PX-9-301 or by the diagram appearing on the front panel of the cycling unit.

+ 4 addition times.

Constant Transmitter and IBM Reader. The IBM reader can read sixteen groups of positive or negative five digit numbers from an IBM card and cause these to be set up on relays in the Constant Transmitter. Four other groups of five digit numbers may be set up on panel three of the Constant Transmitter. Provision has been made for combining these five digit groups to make ten digit groups. When desired, the Constant Transmitter can transmit any of these groups of numbers to various other units of the ENLAC. Transmission of a number by the constant transmitter takes one addition time, but reading and setting up relays to change a number takes longer.

Printer and IBM Gang Punch. The printer can be connected by static cables to eighty decades (and sixteen PM units) located in either accumulators or in the master programmer. When so programmed the printer will cause the IBM punch to punch as many as eighty digits (again associated in groups of five or its multiples for PM purposes) and 16 PM indications on the IBM card. Thus, the numbers registered in these printing accumulators or in certain decades of the Master Programmer can be punched on an IBM card.

Master Programmer. Whole sequences of computations can be arranged locally, that is, by setting switches and plugging cables at the various units of the ENLAC. The master programmer is particularly designed to cause certain sequences of computations to repeat, or to keep track of how many sequences are performed, or by means of digit or sign control to change the sequences when variables reach prescribed values, or combinations of these operations.

1.1.2. Digit Trunks.

A digit tray is about eight feet long and has eleven lines. Ten of these lines carry the pulses representing the ten different digits of a ten digit number and the eleventh carries pulses representing the PM indication.

It takes several trays to extend around to the various units. Several trays connected together with jumper cables and with one load box plugged in forms a digit trunk. These digit trays rest on brackets just above the front panels of the units.

1.1.3. Program Trunks.

Program trays are similar to digit trays except for the type of outlet sockets. Several trays interconnected with jumpers and one load box plugged in constitute a program trunk. The program trays rest below the front panels of the units.

1.1.4. Static Cables

Whenever the decades of an accumulator are connected by static cables to some other unit it means that every stage in every decade and at least one stage of the PM counter is connected to the proper points of the other unit (printer, for example). To accomplish this, two 55 conductor cables are used. In the case of the accumulator to printer connections, only 51 leads of each cable are used, that is, 50 for five decades and the other line for PM indication. An adaptor is used at the accumulator end to connect both PM lines to the M static output of the PM counter. In the case of the static connections to the Master Programmer the PM line is not used, but an adaptor (see 9.2) must be inserted in the printer to keep the PM relays from operating.

1.2. FUNDAMENTAL ELECTRONIC UNITS OF THE ENLAC

There are certain fundamental circuits which are repeated many times throughout the ENLAC. We shall discuss a number of these here. In the course of the following discussion we shall use the terms "pulse" and "gate" with the following meanings:

Pulse: A pulse is a positive or negative change in potential which has a duration of about two to five micro-seconds ($\mu\text{sec.}$)

Gate. A gate is a positive or negative change in potential which has a duration of ten micro-seconds or more. The Carry-Clear Gate (see Figure 306), for example, lasts for 70 micro-seconds.

It will be seen that the same type of electronic units located in different parts of the ENIAC operate at different absolute voltage levels. For example, the flip-flop illustrated (PX-1-105) operates in a voltage range from -555 volts to -360 volts. Other flip-flops operate in ranges of from -85 to +110 volts and from -920 to -725 volts. The power supply produces a range of voltages from -920 volts to +550 volts.

Throughout this report the following convention will be followed with regard to input and output circuits. An input or output will always be represented by only one lead. The return circuit should always be thought of as going back to some point on the bleeder of the power supply. For example, the cathode of a tube may be at zero volts and the output may come from the plate with a range of potential of from 100 volts to 150 volts, say. Instead of using this output with respect to zero it may be used with respect to -20 volts giving an input potential for the next circuit of from 120 volts to 170 volts. Thus, the reference point varies a great deal from circuit through the ENIAC, and it seems impractical to try to represent the return circuits on such diagrams as PX-1-105 to PX-1-110.

1.2.1. Flip-flop.

A flip-flop is a four tube vacuum circuit which is the electronic analogue of an electric switch. Two of the tubes (T_3 and T_4 on PX-1-105) constitute the flip-flop itself, that is, a circuit with two stable states. The other pair of tubes (T_1 and T_2) are called triggering tubes.

The triggering tubes. Assuming that no signal is arriving over the set input, the grid of T_1 is at saturation. This causes the tube to conduct. Thus, if a negative signal of the proper magnitude arrives over the set input the grid will fall below cut-off and the tube will cease to conduct.

In order to secure reliable operation it has been a design principle that in all such cases the grid should be driven three times below cut-off. Furthermore, to provide for the increase in tube resistance with aging, the applied signal has been so arranged that it will always be at least two and one half times below cut-off.

The flip-flop. If the trigger tube T_1 goes off the grid of T_3 will rise well above the cathode potential and T_3 will start conducting. The plate potential of T_3 will drop and this drop in potential will be carried through the condenser C_4 to the grid of T_4 tending to cause T_4 to go off. As T_4 starts to go off its plate potential rises through condenser C_3 this causes the grid of T_3 to rise even faster. Thus, the whole process accelerates. Tube T_3 becomes conducting and T_4 goes off. This being a stable condition, the tube T_3 remains on and T_4 off until such time as trigger tube T_2 goes off.

The output potential at O_1 is -490 volts and of O_2 is -430 volts. After the flip-flop is set by an incoming signal at S the potentials of O_1 and O_2 are interchanged, and they will remain this way until a reset signal arrives at R.

Note that the condensers C_1 and C_2 isolate the DC circuits so the input to the flip-flop may operate at a voltage level which is sometimes as much as 600 volts above the level of the flip-flop.

The general plan will be to connect the outputs O_1 and O_2 to the grids of tubes whose cathodes are at a potential between these two output potentials. For example, in receivers and transceivers these outputs go to the grids of 6SN7's whose cathodes are at -450 volts. Thus, -490 volts is well below cut-off for the one tube whereas -430 volts is far above cut-off for the other one. In this manner static voltages produced by a flip-flop are transmitted to other circuits.

The neon light is visible on the front panel. It is lighted when the flip-flop is set, that is when tube T_3 is conducting.

2.2. Counters

PM Counters. The PM counter is a binary ring counter. That is, it has two stable states and just one input line. A first incoming signal will step it from stage one to stage two whereas the second incoming signal will step it back to stage one. Thus, an even number of pulses arriving over the input line will leave it in its initial condition whereas an odd number leaves it in the other state.

The tubes T_1 and T_2 in PX-1-109 act as triggering tubes. Whenever a positive signal arrives on the input both of these tubes begin to conduct. This causes the grids and plates of both T_3 and T_4 to take a negative swing. Since T_4 is off it has no effect there, but T_3 is caused to go off. As T_3 goes off its plate becomes more positive and through condenser C_3 the grid of T_4 also takes a positive swing. As T_4 begins to conduct its plate takes a negative swing and this through condenser C_2 further causes tube T_3 to go off.

The static output circuits are very similar to the outputs of the flip-flop described above. The positive output has the high potential (relative to the other output) whenever the PM counter is registering a positive number. With tube T_3 conducting and T_4 not (as illustrated) the neon bulb labeled P will be lit and the one labeled N not.

A counter similar to the PM counter is used in the divider-square rooter.

Decade ring counters. A decade ring counter is a ten stage (with two tubes per stage) ring counter with ten different stable states. Each stage has two tubes which will be called respectively tube I and tube II. Only one tube of each stage is conducting. If tube I is conducting that stage will be said to be in state I; if tube II is conducting then that will be said to be in state II. The stable state of the whole ring is with one stage in state I and the other nine stages in state II. The circuits (see the cross

tion PX-5-115 or the decade wiring diagram PX-5-133) are so arranged that one stage is in state I and a pulse is received it will go into state II and the next following stage will go into state I. Pulses that step the ring are negative and are introduced on all the cathodes of the tubes II. This pulse has little effect on the stages in state II but causes the stage in state I to go into state II. As this stage goes from state I to II the carry-over circuit causes the next following stage to go into state I. The fact that this carry-over pulse (through the 50 pf. condenser) will be in conflict with the stepping pulse applied to the cathode requires careful design to obtain reliable operation. Thus, the stepping pulse must be of precise shape and duration, and the carry-over pulse must over-ride it. This is accomplished by putting the incoming pulses through a pulse standardizer (see section 1.2.7.) and by using the proper circuit parameters in the decade ring circuit.

The two cathode resistors for tubes in state I and tubes in state II are so chosen to permit only one mode of operation, namely, one stage in state I and the other nine stages in state II.

Other ring counters. There are a number of other ring counters in the various units of the ENIAC. Essentially they differ from the decade ring counters only in the number of stages they contain. A list of these ring counters follows:

a) The repeater ring. (See PX-5-115) The repeater ring is used in each accumulator to count the number of times a particular repeat program control operates. This ring and its pulse standardizer are built in one plug-in unit. This same plug-in unit is used in the Divider-Square rooter for a different purpose, see (d) below.

b) The cycling unit ring. (See PX-9-307) There is a twenty stage ring counter in the cycling unit which controls what happens during the twenty pulse times of an addition time.

e) The multiplier ring. (See PX-6-308) This ring controls the steps of multiplication. It consists of fourteen stages, ten of which are associated with the ten digits of the multiplier which may be used in multiplication.

d) The divider-square rooter program ring. (See PX-10-304) This ring controls the beginning and final parts of the processes of division or square rooting. It is a nine stage ring which with its pulse standardizer is identical with the repeater ring plug-in units. (see a) above)

e) The divider-square rooter place ring. (See PX-10-304) This ten stage ring keeps track of the place in the division or square rooting process. This ring is identical with the master programmer decade rings (see i) below).

f) The function table argument ring counters. (See PX-7-304) These rings (a units ring of ten stages and a tens ring of eleven stages) receive the argument from an accumulator.

g) The function table program ring. (See PX-7-304) This thirteen stage ring controls the setting up of the function table networks and counts the number of times (up to nine) the functional value may be transmitted.

h) Master programmer decade rings. (See PX-8-304) There are twenty decade rings located on the two panels of the master programmer. These can be used to count the number of times certain sequences of computations are performed.

i) Master programmer stepper rings. (See PX-8-304) There are ten six stage rings which are associated with the ten steppers of the master programmer. These control the output of the program pulses given out by the master programmer.

1.2.3. Gate Tubes.

Besides being able to count and record pulses at high rates it is necessary to control the pulses, switching them into one unit or another. .

In order to do this quickly, electronic switching is used. A vacuum tube used as a switch so as to allow or deny passage of pulses or other signals is known as a gate. Gate tubes are used in the ENIAC for a variety of control purposes. They connect the input channels of any given accumulator to particular digit trays when desired. They are used in the carry-over circuits to pass carry over pulses. Each programming circuit contains many gate tubes.

Most of the gating or switching in the ENIAC is accomplished by the use of multiple grid vacuum tubes. Various gate tube circuits are illustrated on diagram PX-1-106. If there is no input signal to either control grid of the gate tube of PX-1-106, the second control grid is at about -40v. This is well below cut-off for that grid (cut-off is -14 volts for 6Sa7 with the first control grid connected to the cathode). Moreover, the first control grid is at -40 volts which is well below cut-off (-7 volts if second control grid is connected to the cathode), so the tube is not conducting and the potential on the output is near +160 volts. If any positive signal (of about 50 volts) arrives on either control grid the tube will not conduct. Thus, any signal arriving on the first input has no effect. However, if a signal arrives on both grids the tube will conduct and the plate potential will drop. For example, input 2 may connect to the plate of an inverter tube (see section 1.2.6.) which is normally on. If this inverter tube is conducting and the circuit parameters are properly arranged the potential of control grid 2 will be well below cut-off and any signal arriving on control grid 1 will not be passed. When the inverter is off the second control grid is at about +20 volts and any positive signal arriving at the first control grid will be passed.

The resistance and voltages and even the type of tube used in gating circuits varies from circuit to circuit throughout the ENIAC. Various situations are illustrated on the cross sections of the units of the ENIAC.

A gate tube may be called a coincidence tube, since an output will be obtained only if the signals applied to the inputs one and two coincide in

time. Two other types of coincidence circuits used respectively in the Function Table and the Master Programmer are illustrated on PX-1-106.

In the case of the triple coincidence circuit all three of the tubes 1, 2, and 3 must go off before the two control grids of the 807 (tube 4) are sufficiently positive for it to conduct. In the Master Programmer circuit any one of the tubes 2, 3, 4, 5, or 6 being on is sufficient to hold the second control grid potential below cut-off. Thus, the gate (tube 1) will conduct only when there is a positive signal on the first input and the five tubes (2, 3, 4, 5 and 6) are off.

The positive gate potentials which must be supplied to a gate tube for switching purposes can be obtained from the outputs of a flip-flop (see section 1.2.1.). With the proper relationship of supply voltages for the gate tube and the flip-flop one of the outputs of the flip-flop may be connected directly to one of the control grids of the gate tube. The effect obtained is that of a switch which may be opened or closed at desired times by pulses applied to the S or R inputs of the flip-flop.

As a matter of policy the grids are driven to saturation when the tubes are on and they are three to four times below cut-off when off. This means the circuits are not amplitude sensitive, that is, a considerable change in supply potentials and in tube conductance (due to aging) will not effect the reliability of operation. Furthermore, to avoid coincidence problems pulses are never used to gate other pulses; that is, at least one grid of a gate tube is always operated by a gate voltage.

1.2.4. Buffer Tubes.

Many occasions arise in which it is necessary to couple two or more circuits, say, A, B, C, etc., to another circuit, X, so that any one, say A, can operate X without affecting the others, B, C, etc. This can be done by the use of buffer tubes as illustrated on PX-1-107. If such a tube has its grid below cut-off then any change in plate potential will not cause any disturbance

in the potentials of the grid or cathode circuits. Thus, the plates of a number of such tubes (representing the circuits A, B, C, etc.) may be connected together to the input of the circuit X. If the grid of one of these buffer tubes receives a positive signal the tube will go on causing a negative input signal to circuit X. This will cause no disturbance in the grid potentials of the tubes which do not go on. On the other hand no harm is done if more than one buffer tube goes on.

A good illustration of the action of buffer tubes is given on the accumulator cross section PX-5-115. There are eight clear gate buffers (CL. G. B., tube 63) with the plates (CB_T) all connected to the grid of an inverter tube (J50 in the gate unit). If any one of these buffers begins to conduct the potential on all the plates and on the grid of J50 will fall. The only effect will be that J50 will go off. Although the grids of these clear gate buffers are directly connected to the gate tubes 68 in the transceivers, these gates are not disturbed in the other seven transceivers.

1.2.5. Cathode Followers.

A cathode follower is illustrated on PX-1-107. The input of this tube is connected to the plate of an inverter tube which is normally on. This holds the grid potential of the cathode follower below cut-off. If a signal turns this inverter tube off the grid will rise to about 50 volts and the cathode follower will begin to conduct. As the tube goes on the cathode will rise in potential giving a positive output. This rise in potential is limited by the grid potential.

Thus, in the case of a cathode follower a positive input gives a positive output.

1.2.6. Inverter Tubes

If a positive pulse or gate, rather than a negative one, is required (in order to operate another gate tube, for example), then an additional tube must be inserted in the circuit. This tube is known as an "inverter". It is

normally conducting, and when a negative potential is applied to its grid, so as to bias it to cut-off, a positive change in plate potential takes place. This may then be used to operate other tubes, normally non-conducting in the desired way.

The role of a gate tube is that of the logical "and" while a buffer is similar to a logical "or". Arrangements of inverters such as illustrated on PX-1-106 also corresponds to the logical "and".

1.2.7. Pulse Standardizer.

It has been mentioned that in the operation of a counter it is necessary that the input pulses have a certain shape and magnitude. Distortion of pulses because of the capacitance of interconnecting circuits and because of passage through various gate tubes makes it necessary to use pulse-standardizing circuits at the counter input to secure reliable operation. The pulse standardizer circuit includes a flip-flop different from that discussed in 1.2.1. in that one of its states is only semi-stable.

After an input pulse has flipped the circuit, it will flip back to its original state in a time determined by the circuit constants and practically independent of the input pulse. (See PX-1-110).

The explanation of this action is as follows: the values of R_5 , R_6 , and R_7 are such that when tube T_3 is conducting, the current through R_6 biases tube T_2 to cutoff. If a negative pulse is applied to the input, T_1 goes off and tube T_2 is turned on, and the voltage at the plate of tube T_2 drops because of the current through R_4 . This voltage drop is transmitted to the grid of tube T_3 through the capacitor C_1 , and tube T_3 is thereby cut off. However, this negative bias is gradually lost because current then flows through R_5 to the grid and the capacitor C_1 , therefore after a time which depends on the product R_5C_1 , tube T_3 is no longer biased to cut-off; and as it begins to conduct, the increased current through R_6 begins to bias tube T_2 to cut-off again. This change in tube T_2 reacts on tube T_3 , and the action is accelerated, flipping

the circuit back to its original state.

When used to supply properly shaped pulse to a counter this circuit includes a power output tube, T_4 .

Special pulse standardizer. A diagram of the special pulse standardizer appears on PX-1-110. The diagram shows a switch on the input; actually, there are three of these circuits all located in the cycling unit (see PX-9-307). and the respective inputs come from (a) the initiating pulse switch on the front panel of the initiating unit, (b) the reset cam of the IBM punch, and (c) from the finish cam of the IBM reader.

If the switch is closed the condenser C_1 will discharge through the 4.7K resistor. The time constant for this discharging action is slightly more than 2 milliseconds. Thus, the switch should be closed for a period of at least this many milliseconds. As the condenser discharges the grids of tube T_1 drop in potential and the tube goes off.

After the switch is opened the time constant for charging is about 50 milliseconds. Therefore, if the switch were pushed again before the condenser had recharged, the tube T_1 would have not began to conduct again and there would be no output pulse the second time. The time constants here are purposely slow (compared to the speed of operation of the ENIAC) to prevent any chattering of the contacts of the switch (or other transient effects) from causing more than one pulse to be given out.

As tube T_1 goes off its plate potential rises causing tube T_2 to conduct. The flip-flop action of tubes T_2 and T_3 gives a negative pulse to the condenser C_2 causing the tube T_4 to go off. Whether T_2 remains off or not (it will remain off as long as the switch is closed) the grid of T_4 will charge up through the 180K resistors causing the tube to conduct again. The time that tube T_4 is off is, therefore, independent of the length of time that the switch makes contact. Note that releasing the switch causes T_2 to go off

giving a positive signal through the condenser to the grid of T_4 . Since T_4 is already conducting this positive pulse has no effect.

1.2.8. Transmitter

PX-1-108 shows the details of a transmitter circuit. Because of the large capacitances associated with the interconnection circuits, such as digit trays, program trays, and patch cords, it is necessary to use power tubes working into relatively low load resistances in order to transmit pulses from one unit to another at the rate of 100,000 pulses per second. These pulses are positive in order to operate gate tubes and buffer tubes in the accumulators. The diagram of PX-1-108 illustrates the method of achieving this.

The output, or transmitter, tubes have a low resistance in the cathode circuit, 220 ohms. This load resistance is located in a load box and is plugged into a socket in the digit or program trunk into which the transmitter output is fed. The load resistance cannot be connected permanently to the cathodes of the transmitter tubes since depending upon the jumper connections made on the front panel several transmitter tubes may feed into the same line. Thus, just one load box must be plugged into each digit and each program trunk.

The transmitter tubes are normally off. Since the output load is essentially a large capacitance, the positive pulse can be produced quickly only by driving the grids of these output tubes positive with respect to their cathodes. In order to make the output pulse amplitude stable, the grid must be sufficiently positive so as to reach the saturation current for the tube. Considerable grid current will then flow, and it is necessary to provide another tube, known as the driver tube, capable of maintaining the required grid potential under these conditions. The driver tube is actually a smaller power tube. It is normally conducting, and is cut off by a negative pulse input to its grid.

When a signal arrives at the driving tube the grid drops from about -105 volts to approximately -165 volts. This causes the driver tube to go off raising the grid potential of the transmitter tubes. As the transmitters go on the cathode potential rises to about 45 volts.

The digit outputs of the divider and multiplier do not have standard transmitters. They have inverter tubes with built in load resistances. Thus, the lines that these tubes feed into must not have load boxes and for reliable operation the pulses should not be fed into a transmission system exceeding the loading rules stated in the operator's manual.

1.2.9. Receiver Plug-in Unit:

The wiring details of a receiver appear on the accumulator cross section (PX-5-115 while a block diagram representation of the receiver appears on PX-5-304 (accumulator block diagram). For a detail wiring diagram of a receiver plug-in unit the reader is referred to PX-5-148.

The incoming signal arrives at a buffer (tube 66) turning it on. This causes a drop in the plate potential, that is, this tube inverts the signal. The negative output of this buffer is used to set the flip-flop (64, 65 say). The positive (that is, positive after initial clearing) output of the flip-flop feeds into what is called a fast buffer output (62 and 63). This is an inverter (62) operating a cathode follower (63). The inverter is normally on. When the flip-flop is set the decrease in potential on the output turns the inverter off and the cathode follower on. This gives a positive gate on the output. The normally negative output of the flip-flop goes to a buffer tube (62) forming what is called the slow buffer output. The time constant for this output is much longer than that of the so called fast buffer output; this explains the terminology.

The negative output of the flip-flop also goes to the grid of a gate tube (61). When the flip-flop is set this gate can pass a reset signal causing the flip-flop to reset. In the case of receivers used in the accumu-

lators the other grid of this gate is connected to the central program pulse (CPP) line. Since the set signal is usually a CPP gated at some other unit of the ENIAC the receiver will start to come on at about pulse time 17 (or slightly later depending upon the time constants of the intervening path) of one addition time. At pulse time 17 of the next addition time the reset gate (the time constants are such that this does not open in time to pass a resetting CPP which would conflict with the setting program pulse) pass a CPP which resets the flip-flop. Thus, the receiver is on for one addition time. In other units (in particular, in the divider and multiplier) the reset pulse passes through other gates which allow the receiver to remain on more than one addition time.

1.2.10. Transceiver Plug-in Unit.

As with the receiver the wiring details of a transceiver appear on the accumulator cross section PX-5-115 and a block diagram representation appears on the accumulator block diagram PX-5-304. For a detailed wiring diagram of a transceiver the reader is referred to PX-5-147.

As far as the fast buffer output is concerned the transceiver is identical with a receiver. On the normally negative output of the flip-flop are two buffers (61) giving two slow buffer outputs. This line also feeds a reset gate (62). The output of the reset gate goes through an inverter (65) to two more buffer outputs (63) and to a gate (68) which passes a CPP. The CPP passed by this gate resets the flip-flop and goes through a transmitter.

The usual mode of operation is as follows. An incoming program pulse goes through a buffer (69) and sets the flip-flop. The gates provided by the fast and slow buffer outputs are used to cause the unit to perform a certain task. When the task is finished a signal arrives at the gate opened by the normally negative (now positive) output of the flip-flop. The gate passes this signal turning off an inverter giving two more output gate signals

and opening another gate to pass a CPP. This CPP resets the flip-flop and is transmitted (via cables and program trunk) to some other unit to program the next step in the computation. The delayed buffers (63) furnish gate signals which may perform the final parts of an operation such as the case of an accumulator.

1.3. BLOCK AND CROSS SECTION DIAGRAMS.

Chapters II to X are devoted to descriptions of the various units of the ENIAC. The descriptions of the units will, in general, be given in terms of block diagrams and cross section diagrams. A block diagram uses circles and rectangles to represent various electronic devices, and has the following purposes:

- 1) to aid in understanding the various circuits and their operation without going into details.
- 2) to enable people with computational problems to understand the ENIAC sufficiently (irrespective of their electronic background) so as to adapt their problems to it.
- 3) to assist the maintenance man in finding mechanical and electrical failures.

Cross section diagrams give typical circuits in all detail, that is, all resistors, condensers, inductances, tubes, all voltages, et cetera, are given. If a unit contains many circuits which are practically identical, only one appears on the cross section. The cross sections have the following purposes:

- 1) to enable the person with an electronic background to understand in detail how the ENIAC operates.
- 2) to assist the service man in making proper replacements of parts.

As a general practice in the following chapters, programming details (switch settings and plugging of interconnectors) will be described only to the extent required to understand the circuits. For more detailed programming and

illustrative set-ups the reader is referred to the corresponding chapter and sections of part I of this report.

As standard practice on all block diagrams the following conventions will be followed:

- 1) Broken lines indicate pulse carrying lines while solid lines carry gates.
- 2) Tubes (except for stages of rings and pulse standardizers) which are normally conducting are shaded, others not. The word "normally" here means immediately after initially clearing, or in the case of the cycling unit, the situation which exists when the ring is at stage zero and no pulse is coming from the oscillator.
- 3) Plug-in units will be represented by rectangles with heavy borders.

II. INITIATING UNIT

The initiating unit, as the name implies, contains the controls which start and stop (turn on and turn off the power) the ENIAC. There is a push button on the initiating unit front panel (see PX-9-302) which initially clears the ENIAC, that is, it clears all decades to their zero stage, clears PL rings to their first (P) stage, repeater rings to stage one, and program controls to their unactivated state, and so forth. The program terminals and controls for the IBM reader and punch are located on this panel. From these controls program pulses can cause the reader to read a new card, or the printer to print the numbers registered in certain accumulators and possibly some decades of the master programmer. Also there is a push button by which the reader may be caused to read a new card. When the card reading is finished and an interlock signal has arrived, a program pulse is given out from one of the terminals on the front panel (see PX-9-302, terminal R₀). The interlock signal is a program pulse indicating the ENIAC has finished some other sequence of computations which was going on simultaneously with the card reading. In manual operation, by the push button, no interlock signal is needed. Likewise, when the printer relays have set at the beginning of the card punching cycle a program pulse is obtained from a terminal on the front panel (terminal F₀). These pulses can be carried over lines of a program trunk to some other unit of the ENIAC, causing some other operation to take place. There is another push button which produces what is called an initiating pulse (at terminal I₀) that can be used similarly to the reader and printer program output pulses. There are six

program input and output terminals (C_1 and C_0 on PX-9-302) associated with six transceivers which transmit the selective clear gate over the cycling unit trunk. This selective clear gate (SCG) goes to each of the twenty accumulators and causes those which are so set (set to selective clear) to clear. There is another push button which shunts out the door switches and allows the E. L. C. to be operated with the doors of some of the units off, this is called the door switch shunt.

2.1 STARTING AND STOPPING SEQUENCE AND INITIAL CLEAR

The following descriptions will be given in terms of diagrams PX-1-101 (Power and control wiring for the EMLC) and PX-9-307 (Cycling unit and initiating unit block diagram). The right hand portion of PX-9-307 shows the circuits located either in the initiating unit or on the switching and fuse panels. The left hand portion shows the circuits of the cycling unit.

2.1.1 Normal Initial Conditions

The normal state with the EMLC turned off is to have relays C and H (see the simplified control circuits on upper right corner of PX-1-101 or see the lower right hand corner of PX-9-307) activated.

In series with relay C are 46 door switches (shunted out by the door switch shunt - see PX-9-302), and 43 thermostats. If any one of these 89 contacts is open then relay C will be unactivated, and, as explained below, this makes it impossible to turn the EMLC on. The thermostats are located in the tops of the various units which contain vacuum tubes. If the temperature of any one of these units rises above 115° the corresponding thermostat contact will open and turn the EMLC

off or prevent it from being turned on (until the unit cools down). When the doors are off of the backs of the various units a person is exposed to voltage differences amounting to as much as 1500 volts. Each such door operates a door switch which will cause relay C to drop out (unless the door switch shunt is operated)

When relay C_1 drops out the P timer starts (this timer may be set to run from 0 to 15 minutes before it closes its contact P_1). During the period that the timer is running, a bell will ring to indicate that this timer is about to turn the ENIAC off (if it has been turned on). This turning off is accomplished by opening contact P_1 which opens the holding circuit of the auxiliary relay A. This in turn causes all the contactors and certain auxiliary relays to drop out shutting off all power (d-c and heater) to the ENIAC.

Thus, if a thermostat opens the circuit, or if the back cover is removed opening a door switch (when the door switch shunt is not operated) the P timer starts, a bell rings, and at the end of the period (0 to 15 minutes), all power is shut off from the ENIAC. This time interval gives the operator time to perhaps correct the fault (for example, check the ventilation system) before the power goes off. This system is designed to minimize the number of times the heaters are turned off and on since this turning off and on has been found to cause numerous tube failures (burned out heaters and heater-cathode shorts).

The relay N has in series with it the power supply heater phase failure relays (3 relays), the power supply phase failure relays (3 relays), and the under voltage release relays (28 relays). All these contacts are open when the power is off, thus, a contact on relay K (contact K_2) shunts these circuits until relay K is activated. Since relay K is not activated

until a minute and ten seconds after the start button is operated or ten seconds after the d-c power comes on, this allows the under voltage release relays and the phase failure relays to pick up. In other words, there is no undervoltage or phase failure protection during this ten second interval. If there is an undervoltage (because of failure in some power supply) or a phase failure, then one of these relays will drop out (or not be picked up when the machine is started) and the relay N will drop out when relay A is activated. As explained below this will shut off the plate supply to the power supplies, and consequently turns off the d-c to the ENLAC. This leaves all the heater voltages on but turns off the d-c.

2.1.2 Complete Starting Sequence

(1) Push start push button (on initiating unit front panel, PX-9-302).

Relay A is activated (assuming relay C is activated).

Contactors B is activated by a contact on relay A. This turns on the ENLAC heaters picking up the heater phase failure relays (6 relays). Relay A is now held by contacts F_1 and B_1 . Contactor B is held by contacts A_1 and B_1 .

The start pilot (amber light on initiating unit front panel) and the power supply time recorder (on initiating unit front panel, tells total time that the power supply heaters have been on) are turned on by contact A_4 on relay A. If any d-c fuses are blown then a circuit through contact A_4 and a contact on one of the d-c fuse relays causes relay L to pick up. This would prevent the d-c power from being turned on by preventing contactor G from being activated. If any of the power supply

Filament fuses are blown the relay Q will pick up and hold on contact Q₂.

Contactor E is picked up by contact A₃ on relay A. This supplies power to the fans in the ventilating system.

Contactor D is picked up by contact E₁ on contactor E (assuming that relay Q is inactivated). This furnishes power to the power supply heaters.

The one-minute timer F is started by a contact D₁ on contactor D provided heater phase failure relays have picked up. This timer runs for one minute and then the contact labelled F₁ is closed. This contact remains closed as long as power is applied to the timer, that is, as long as contactor D is activated. Whenever power is removed the contacts open and the timer resets itself.

After one minute the power supply contactor G is picked up by the timer contact F₁ (assuming relay L is not activated). This contact furnishes power to the plates of the rectifiers in the power supply and thus furnishes d-c power to the EMERG.

Relays H and K and the ten second timer J are picked up by contact G₁ on contactor G. The initial clear relay No. 1 (H) operates certain relays in the initiating unit which produce the initial clear gate (ICG) (see Section 2.1.2). The 14 undervoltage release pick-up relays L shunt the resistances in series with the coils of the undervoltage release relays. Since the drop-out point for a relay is considerably below the pick-up point the resistances in series with the coils are adjusted so that a small drop in voltage from one of the power supplies will cause the relay to drop out and thus shut off the d-c power (by releasing relay H which picks up relay L). The pick-up point is then too

high for these relays to be picked up by the voltage from the power supplies. Thus, for a period of ten seconds (during the running of the ten second timer) the relays H cause these resistances to be shunted with smaller resistances to enable the relays to pick-up.

Ten seconds later the contact J_1 closes on the ten second timer. This causes relay K to pick up. Relay K holds on a circuit through contacts G_1 , K_1 , and the initial clear push button. When relay K is activated, contact K_4 opens, releasing relays H and K , and allowing the timer J to reset. Contact K_2 opens applying the phase failure and under voltage protection (since relay H is also released). Contact K_3 closes turning on the ready pilot (green light on initiating unit panel).

The green light indicates that the power is on and that the ENIAC has been initially cleared (as described in Section 2.1.2) and is ready to start computations.

2.1.3 The d-c off Sequence

Push the d-c stop button. This causes relay L to be activated. Relay L remains activated by circuit through d-c start button and holding contact L_2 . Contact L_1 opens dropping contactor G . This shuts off the plate supply to the power supply and thus shuts off the d-c to the ENIAC. Contact G_1 opens dropping relay K (this puts the initial clear circuits into their normal initial state).

If a d-c fuse blows, one of the d-c fuse relays will pick up. This will activate relay L and have the same effect as pushing the d-c stop button. If the voltage from any one of the various power supplies is subnormal, one of the undervoltage release relays will drop out. If there is a phase failure in the voltage to either the ENIAC heaters or to

the power supply heaters or plates one of the phase failure relays will drop out. In any of these last cases relay N will drop out closing the contact N_1 . This, again, has the same effect as pushing the d-c stop button.

Frequent turning off and on of the heaters of the tubes is undesirable because this tends to increase the number of heater failures. Thus, the d-c on and off circuits are provided so that the heaters may be left on continuously while the d-c can be turned off when the machine is not in use or when parts must be replaced.

A locking arrangement is provided so that personnel may padlock the d-c start and stop buttons and prevent anyone from turning on the d-c while someone is working on the machine.

Should one of the power supply heater fuses blow, one of the three power supply heater fuse relays will operate. This will pick up relay Q, which by opening the contact Q_1 , will turn off all power to the power supply. (Contactor D will be deactivated removing heater power. Timer contact F will open since contact D_1 has opened deenergizing timer F, and hence the plate supply through contactor G will also be turned off). With power supply heaters deenergized it is safe to replace a heater alarm fuse, although it is recommended that additional precaution be taken by opening safety disconnect switch which has been provided. If the safety disconnect switch is used, it must be again closed before attempting to turn on the d-c power.

2.1.4 The d-c on Sequence

Push the d-c start button. This causes relay L to drop out. The d-c contactor G is picked up by a circuit through contacts F_1 and L_1 .

The rest of the sequence is exactly like the last part of the sequence described above (see Section 2.1.2).

If the power supply a-c and d-c has been turned off from a master fuse failure, pushing the d-c start button will turn it on since relay Q will be released permitting contactor D to pick-up through Q₁. The rest of the sequence is exactly like the last part of the sequence described above (Section 2.1.2). It should be noted that when relay Q trips off the d-c, an extra one minute (over a relay L tripping) will elapse between the pushing of the d-c start button and the initially cleared signal since timer F is now introducing tube warm-up delay.

2.1.5 The Initial Clear

Near the end of the starting sequence (see Section 2.1.2) relay H is activated during the period that the ten second timer J is running. Thus, for a period of ten seconds initial clear relay No. 3 (in the initiating unit) is activated by a circuit through contact H₁. This changes the potential on the screens of certain gates in the master programmer from +150 volts to zero volts (this is called the master programmer clear - IPC). This change in potential prevents the corresponding gates from conducting and, thus, during this ten second period no program pulses are transmitted from the master programmer. For a more complete description of this situation see Section 10.3.2.

Another contact on initial clear relay No. 3 opens allowing a 125 mf. condenser to charge up during the ten second interval. At the end of the ten second interval relay K is picked up by the contact J₁. Contact K₄ opens dropping relays H and L and allowing the ten second timer J to reset. As H drops initial clear relay number three drops

changing the bias on the screens of the gates in the master programmer (MPC) back to +150 volts. Another contact on this relay closes allowing the 125 mf. condenser to discharge through the coil of initial clear relay No. 4. This relay is activated for a period of about one second and changes the potential on the initial clear line from -345 volts to -290 volts. This produces the initial clear gate (ICG). This initial clear line goes around to the various units by way of the d-c wiring channel.

The initial clear circuits work automatically at the end of a starting sequence or with a d-c on sequence. The initial clear sequence also takes place when the initial clear push button is operated (on front panel of the initiating unit, see PX-9-302).

There follows a list of things which take place in the various units during the process of initially clearing.

(1) Initiating Unit (see PX-9-307).

The initial clear gate (ICG) three gates which pass central program pulses (CPP) which reset the reader and printer start flip-flops (65, 66, and 68, 69 on PX-9-104) and the reader interlock, reader finish, and the reader synchronizing flip-flops (67, 68 and 70, 71 on PX-9-103 and 63, 64 on PX-9-106). (See sections 8.2 and 9.1.2.)

(2) Cycling Unit (PX-9-307).

The initial clear gate is not used in the cycling unit.

(3) Accumulator (PX-5-304).

The ICG gates central program pulses which cause the decades and the PM counter to clear back to their first stages (or possibly some decade may clear to five for round-off purposes) and the repeater ring

(associated with the transceivers) to clear back to stage one. (See Sections 4.2.3 and 4.1.2.)

(4) High Speed Multiplier (PX-3-308).

Here the ICG gates central program pulses which step the program ring to stage one (see Section 5.3) and which reset the l and r receivers (which control the product accumulators in the process of receiving the partial products).

(5) Divider and Square Rootor (PX-10-304).

The ICG gates central program pulses producing C1 and C1' pulses which perform the clearing actions as described in Section 6.2.9. Actually these pulses clear the program ring, the quotient place ring, and the numerator binary ring, and reset numerous flip-flops.

(6) Function Table (PX-7-304).

The ICG gates central program pulses which clear the argument rings, the program ring and resets certain flip-flops (see Section 7.4.4).

(7) Constant Transmitter (PX-11-307).

The ICG is used only in the reader control circuits which are located in the initiating unit, see (1) above.

(8) Printer (PX-12-307).

The ICG is used only in the IBM punch control circuits which are located in the initiating unit, see (1) above.

(9) Master Programmer (PX-8-304)

The ICG gates central program pulses which clear the decade rings and the stepper rings (see Sections 10.2.1 and 10.3.1).

If any program pulses get started in the trays and jumpers which extend around the machine (they might get started when the d-c

power comes since certain flip-flops may come on in the set or abnormal position) they will run out any sequence which an operator has plugged in. However, if any of these sequences pass through the master programmer the pulses will not pass here during the initial clear period (because the master programmer clear (MPC) blocks the program output gates, see Section 10.3.2. The period during which the initial clear is on is ample (including a safety factor) for any manually plugged sequences to run out (assuming that no one has plugged in any complete cycles of programs which do not pass through the master programmer). Then, after the initial clear sequence is completed (and the ready pilot goes on) the machine is ready to start any sequence of computations which may be programmed.

2.2 INITIATING PULSE PROGRAM CONTROL

The initiating pulse plug-in unit is activated by a push button and produces a program pulse which is synchronized with the ENIAC. This pulse appears at a terminal I_0 on the front panel (PX-9-302) and can be carried around the program trunk system to any unit of the ENIAC.

This unit is pictured in the upper right hand corner of PX-9-307. Closing the initiating pulse push button causes the special pulse standardizer (tubes 61 and 62) to set the flip-flop (64 and 65). This opens the gate 66 which passes a central program pulse (coming from the cycling trunk) setting flip-flop 67 and 68. This flip-flop opens gate 69 passing a CPP which resets both flip-flops and goes through the transmitter to the output terminal I_0 (see PX-9-302) on the front panel.

The two flip-flops operating as described above always provide a standard output program pulse. Gate 66 may open in such a way that only part of a CPP is passed. If it fails to operate flip-flop 67 and 68 no harm is done since flip-flop 64 and 65 is not reset and the next CPP is passed full strength by gate 66. Then the flip-flop 67 and 68 has one full addition time in which to set up so gate 69 is open and passes a standard program pulse. This pulse then resets the flip-flops and is transmitted.

There is no cross section diagram of this circuit. Clearly, since there is no parallelism of circuits in this unit, a cross section must be as detailed as the actual wiring diagram of the circuit. The number PX-9-105 in the corner of the drawing of the plug-in unit refers to the wiring diagram.

2.3 OTHER FEATURES

2.3.1 Selective Clear Controls

There are six transceivers located in the initiating unit with program input and output terminals on the front panel. The output of the cathode followers of the respective transceivers is connected to a line of the cycling trunk and provides the selective clear gate (SCG). This gate is used to clear any of the twenty accumulators depending upon the settings of their selective clear switches (see Section 4.2.3).

Thus, whenever a program pulse enters one of the terminals C_1 the selective clear gate is provided for a period of one addition time and a program pulse is transmitted out of the terminal C_0 at the end of the addition time. These transceivers are reset by a CPP after one addi-

tion time. A more detailed block diagram representation of a transceiver appears on PX-5-304.

2.3.2 Reader and Printer Program Controls

Control circuits for the IBM reader and the IBM ~~gang~~ punch are located on plug-in units (see the four plug-in units below the initiating pulse plug-in unit on PX-9-307) located in the initiating unit.

These circuits are described in detail in the discussion of the constant transmitter (Chapter VIII) and of the printer (Chapter IX).

2.4 TESTING FEATURES

On the front panel of the initiating unit there appears a hum oscilloscope, an a-c voltmeter, and a d-c voltmeter. These are used to check the amount of hum on the a-c power lines supplying the EMIAC, the voltages on the three phase lines supply the a-c power, and the d-c voltages put out by the power supply. Two switches enable the operator to check every d-c voltage used in the machine. A table of proper values and tolerances appears on this panel.

For a complete discussion of testing procedures, et cetera, the reader is referred to the maintenance manual (part III of this report).

III. CYCLING UNIT

The cycling unit produces the pulses which are used to represent digits and to control the operation of units of the ENIAC. Also the carry-clear gate (CCG) is produced in the cycling unit. The pulses produced in the cycling unit control the timing of the operations and enables the various units to operate in synchronism.

The following table gives a list of the pulses or gates produced in the cycling unit. Also appearing in the table is the principle purpose of each pulse or gate.

TABLE 3-1

Pulse or gate	Abbreviation	Purpose
Central Program pulse	CPP	A program pulse used to control the activity of the various units of the ENIAC.
Tens pulses (off beat)	10P	Used to cycle the decades of the accumulator during the process of transmission of the number (or its complement) registered in the accumulator.
One pulse	1P	A coded system in the multiplier, function tables, and the constant transmitter makes use of combinations of these pulses to represent the digits zero to nine.
Two pulses	2P	
Two-primed pulses	2'P	
Four pulses	4P	
Nine Pulses	9P	Some of these pulses are used to represent the digits zero to nine.
One-primed pulse	1'P	In the process of taking the complement this pulse is used to obtain the complement with respect to 10^n instead of 10^{n-1} .
Reset pulse	RP	This pulse is used to reset flip-flops in the accumulator decade units and to provide a carry-over pulse in the process of addition.
Carry-clear gate	CCG	This gate controls the carry over process when adding in an accumulator and produces the clearing action when so desired.

The pulses and gates listed in the table above are produced in the cycling unit once each addition time. PX-9-306 shows the temporal order of these pulses and gates. These pulses and gates along with the selective clear gate from the initiating unit (see 2.3.1.) are distributed around to each unit of the EELAC by the cycling trunk.

An addition time is normally 200 micro-seconds long. Each addition time is divided into twenty parts called pulse times, each ten micro-seconds long. All of the pulses except the 10P are produced at the beginning of a pulse time and all have a duration of about two micro-seconds. The tens pulses (10P) pass through a 2.5 micro-second delay line and thus arrive at the beginning of the second quarter of a pulse time. The tens pulses, 10P, are used to cycle decades in the accumulators (see 4.3.) during the process of transmitting the contents of the accumulator. These off-beat pulses are produced 2.5 micro-seconds late for timing reasons which will be explained in the chapter on the accumulator (see 4.3.1.).

3.0. INTRODUCTION

The block diagram of the cycling unit along with that of the initiating unit appears on PX-9-307. In the upper left corner is the oscillator plug-in unit. To the right of this are the relays which determine the mode of operation: continuous, one addition time, or one pulse time. Below the oscillator plug-in unit are two more plug-in units containing pulse standardizers and delay lines. Near the middle is the twenty stage ring which counts out the pulse times of an addition time. Below the ring are pulse gates, then the amplifiers, and finally the transmitter plug-in units. The outputs of the transmitter plug-in

units go to the cycling unit trunk which carries the various pulses and gates around to each unit of the ENIAC.

3.1. THE OSCILLATOR AND PULSE FORMERS.

3.1.1. The Oscillator

The crystal oscillator always oscillates at a frequency of 100 kilocycles. Whether or not the output of the oscillator is used depends upon the setting of the external oscillator switch and the continuous and one addition time relays. The socket and the external oscillator switch makes it possible to operate the ENIAC with an external oscillator, and, more important, to operate the ENIAC at different frequencies for purposes of checking (for example, to check safety factors).

Note: If the ENIAC is operated at a frequency exceeding 100 kilocycles the safety factors may be lost and reliable operation cannot be expected.

The continuous and one addition time relays cause the oscillator (external or internal) to be connected through the pulse standardizer K-L 26 to the gates L27 and L28 for continuous and one addition time but not for one pulse time operation. Of the three modes of operation the first (continuous) is the normal mode and the following description will be in terms of this mode. The other two modes (one addition time and one pulse time) are for purposes of checking and will be described in section 3.3.

When the continuous relay is activated the cathode circuit of tube 70 is opened, thus turning tube (70) off and, therefore, opening gate L28. That is, since tube 70 is not conducting the plate potential is relatively high; and, therefore, one of the control grids of the gate L28 is sufficiently high

that any positive signal on the other grid will cause it to conduct. Hence, the output of the oscillator goes through the contacts on the continuous relay to the pulse standardizer K-L 26 and through the gate L 28 to the on-beat plug-in unit.

The pulse forming circuit, composed of a special pulse standardizer (tubes 68, and 69, see section 1.2.7.) and tube 70, serves no other purpose than that described above in continuous operation. Its role in one addition time and one pulse time operation will be described in 3.3.

3.1.3. The on-beat plug-in unit

Tubes 61, 62, 63 of the on-beat unit constitute a pulse standardizer. This circuit differs from the usual pulse standardizer in that it has a one micro-second delay line on the plate supply of tube 62. By reflection this delay line helps to produce a square pulse with a length of two micro-seconds.

The output of tube 63 goes to tubes 68 and 67 and thence to a socket located underneath the front panel. Thus, pulses (which are in phase with the nine pulses 9P) arrive at this terminal in the following ways:

- a) for continuous operation one pulse each pulse time,
- b) for one addition time operation twenty pulses (one each pulse time) each time the push button is operated, and
- c) for one pulse time operation one pulse each time the push button is operated.

The output of tube 63 also goes to tubes 65, 64, and 66 and on to the pulse gates controlled by the ring. These pulses are gated by the ring to produce all pulses sent out by the cycling unit except the tens pulses (10P).

The third output of tube 63 goes to the off-beat pulse former plug-in unit and enters a 2.5 micro-second delay line.

3.1.4. The off-beat plug-in unit

From a center tap on the 2.5 second delay line pulses go through a pulse standardizer (tubes 67, 68, 69, and 70) and thence to step the ring. This pulse standardizer is similar to the usual pulse standardizer (used in accumulators) except that it has two driving tubes (67 and 68) operating in parallel.

The end output of the delay line goes through another pulse standardizer to the tens pulses gate L30. This pulse standardizer also has a one micro-second delay line to obtain square pulses of 2 micro-second length.

The pulses which step the ring arrive 1.25 micro-seconds after those that go to the pulse gates which are opened and closed by the stages of the ring. This means that the ring has 8.75 micro-seconds in which to step from one stage to the next, and for reliable operation the ring is designed to step to the next position in appreciably less time than this.

3.2. THE RING AND ITS ASSOCIATED GATES AND FLIP-FLOPS

3.2.1. The tens pulses (10P)

When the ring is on stage 0 gate K27 is open. Thus the first pulse of the addition time passes K27 and sets the flip-flop L29. This flip-flop must open gate L30 inside of 2.5 micro-seconds in order to pass the first of the tens pulses arriving from tube 61 in the off-beat pulse former. Thus, this is not a standard flip-flop; that is, the triggering tubes are omitted in order to improve the time constant. Also, the output time constant is less than for a standard flip-flop.

The output of gate K27 also goes to trigger the scope which is

located on the cycling unit. This gives one addition time sweeps on the scope.

The flip-flop L29 remains set until the ring reaches stage ten. At that time the output of gate A30 resets the flip-flop. Note that in order to not pass more than ten pulses the flip-flop must reset in less than 2.5 micro-seconds.

The output of L30 goes to a two stage amplifier (L41 to L46) and thence to two transmitter plug-in units. A transmitter consists of two stages with five tubes operating in parallel in each stage.

3.2.2. The 1, 2, 2', 4 and 9 pulses.

The one pulse (1P)

When the ring is at stage one gate K30 is opened to pass a one pulse. The pulse goes through an amplifier system (K41, K42, K43, K44, K46, and K47) to a transmitter plug-in unit.

The two pulses (2P).

Stages two and three of the ring open gates J30 and H30 to pass pulses to form the two pulses. After being preamplified by J41, J42, H41, and H42 they are combined and further amplified by J43, J44, J46, and J47, and then fed to a transmitter plug-in unit.

The two-primed pulses (2'P)

Stages four and five open gates G30 and F30 which pass pulses to make up the two-primed pulses. As with the two pulses these are amplified and taken to a transmitter plug-in unit.

The four pulses (4P).

Stages six, seven, eight, and nine open gates E30, D30, C30, and B30 to pass pulses which make up the four pulses. These are amplified and taken to a transmitter plug-in unit.

The nine pulses (9P)

The one, two, two-primed, and four pulses are taken to buffers J45, J45, G45, and E45 and then combined to make up the nine pulses. Then they pass through a two stage (six tubes in parallel) amplifier (A 24 and 25 to F24 and 25) and then to four transmitter plug-in units.

3.2.3. The one-primed pulse (1'P).

Stage ten opens two gates A30 and A27. Gate A30 passes a pulse which resets the tens pulse flip-flop. Gate A27 passes the one-primed pulse through amplifiers A26, B26, A23 to E23 and F23 to K23 and then to three transmitter plug-in units.

3.2.4. The carry clear gate (CCG)

Stage eleven of the ring opens gate B27. This gate passes a pulse which sets the flip-flop E27. The negative output of the flip-flop goes through amplifier tubes D26 and D27 to a transmitter plug-in unit. When this flip-flop is set this output takes a positive swing and the transmitter gives a positive gate on its output. Note that this amplifier system is direct coupled all the way through. The carry-clear flip-flop is reset when the ring reaches stage eighteen. The length of this carry-clear gate (70 micro-seconds) is about $1 \frac{3}{4}$ times that needed for carry over in a twenty decade accumulator, that is, when the carry over takes place there may be a string of carry overs from the first decade down to the twentieth. This gives a seven to four safety factor which is somewhat less than the two to one which is attained in most parts of the ENIAC.

3.2.5. The reset pulse (RP)

Stages 12, 14, 15, and 16 of the ring do not operate any gates. Stage 13 opens gate C27 and passes a reset pulse. Stage 19 opens gate J27 which also passes a reset pulse. Thus, in each addition time there are two reset pulses, one when the ring is at stage 13 and another when it is at stage 19. The output of the gates C27 and J27 goes to an amplifier system H26, G26, G to J 24 and 25. The output of this amplifier goes to three transmitter plug-in units.

3.2.6. The central program pulse (CPP)

Stage 17 opens gate G27 which passes the central program pulse. Since this pulse is used more places by far than any other pulse in the ENIAC it goes through the largest amplifier system. This pulse goes through tubes F27, F26 and E26, then to a two stage (ten tubes in parallel) amplifier (A22 to K22 and A21 to K21). The output now goes to nine transmitter plug-in units which constitutes a two stage amplifier with forty-five tubes in parallel in each stage.

3.3. ONE PULSE AND ONE ADDITION TIME OPERATION

These two modes of operation are provided for purposes of checking the operation of the ENIAC and to check the set-up of the problem. If the answer to a check problem is not correct then it becomes a matter of isolating the fault. This generally can be done by operation in the one addition time mode. Then, operation in the one pulse time mode will generally further help to diagnose the fault. For further discussion on these points see part I of this report.

3.3.1. One addition time operation

In this case the transfer contact on the continuous relay holds the cathode of tube 70 (in the oscillator unit) at -40 volts. This tube is normally on and will go off only upon receiving a negative signal from tube 69 which gets its stimulus from the push button.

The length of this pulse sent to gate L28 must be long enough to be sure to let a pulse from the oscillator through (at least ten microseconds). This first pulse which passes gate L28 steps the ring from stage zero to stage one. Since one of the control grids of gate L27 is connected to the negative static output of stage zero, gate L27 is opened as long as the ring is not at stage zero. Thus, the pulses from the oscillator (via K-L 26) continue to step the ring until it reaches stage zero again. Hence, each time the one pulse or one addition time switch is pushed the ring cycles through all twenty stages and the cycling unit gives out the various combinations of pulses which represent one addition time. Note that the pulse sent to gate L28 by 70 must not last as much as one addition time or else operating the one addition time push button may cause the ring to cycle twice.

3.3.2. One pulse time operation.

In this case neither the continuous relay nor the one addition time relay are activated. This means that the oscillator output is not connected at all. The output of the first triode of 70 goes both to the second triode and to gate L28. The output of the second triode goes through contacts on the one addition time relay and the continuous relay to the pulse standardizer K-L26 and through the gate L28. Thus, each time the push button is operated one pulse is fed into the on beat plug-in unit.

The wide pulse from tube 70 which is applied to gate L28 is delayed (because of the time constants of the path through the relay and the pulse standardizer) and differentiated (narrowed) by the pulse standardizer circuit. This assures its being gated at L28 by the wide pulse from tube 70 on the other control grid.

IV. ACCUMULATOR.

An accumulator is a unit of the ENIAC which is capable of performing the following operations:

- 1) Storing a ten digit number along with the proper indication of its sign.
- 2) Receiving numbers (positive or negative) from other units of the ENIAC and adding them to numbers already stored, properly indicating the sign of the sum.
- 3) Rounding off its contents to a previously determined number of places.
- 4) Transmitting the number held, or its complement with respect to 10^{10} , without losing its contents (this makes it possible to add and/or subtract from the contents of one accumulator those of another).
- 5) Clear its contents to zero (except for a possible round off five, see 4.2.3.).
- 6) Information stored in certain accumulators may be transmitted statically to certain other units (see Section 1.1.4.)

The registering of ten digit numbers is accomplished by the use of decade ring counters (See 1.2.2.) and a PM (plus-minus) counter. The circuits which carry the various groups of pulses representing numbers and signs (including the decade plug-in units and the PM-Clear plug-in unit except for the clear tubes) will be called the numerical circuits. The accumulator contains common programming circuits which in each operation of the accumulator determine which of the above listed operations the unit performs. The accumulator contains a number of program control circuits (eight repeat program control circuits and four non-repeat program control circuits) which can be used at various times to cause the common programming circuits to make the

accumulator perform one of the above operations.

Thus, usually each program control circuit will be used at most once in each sequence of computations whereas portions of the common programming circuits are used each time the accumulator performs an operation. No two program controls are used simultaneously. Actually by making use of the master programmer it is possible to use one program control circuit several times in a given sequence of computations. The operation performed by the numerical circuits (controlled by the common programming circuits) is determined by the various switch settings of the particular program control used.

When activated by an incoming program pulse (arriving via jumper connections from program trays to the accumulator front panel) the program control circuit provides certain gates to the common programming circuits which in turn supply certain gates or pulses to the numerical circuits and thus cause the accumulator to perform a certain operation. At the end of the operation (which may last as many as nine addition times if a repeat program control circuit is used) the program control circuit gives out a program pulse which may be taken to other units of the ENIAC causing them to perform the next step in the sequence of computations.

4.0. INTRODUCTION.

This description of an accumulator will be given in terms of the block diagram PX-5-304 and the cross-section diagram PX-5-115. In the upper center and upper right of the block diagram there are eleven rectangles representing the ten decade plug-in units and the PM-clear unit (on the left). Just to the left of the PM-clear unit are seen the five decks of the significant figure switch. In the lower left hand corner are seen one receiver plug-in unit and two transceiver plug-in units. As indicated on the drawing there is one other receiver plug-in unit and six other transceivers making a total of four receivers located on two plug-in units and eight transceivers

each located on a separate plug-in unit. Just above the code block and below the decade units are the α , β , γ , δ , and ϵ input gates of which only α and ϵ are shown in detail.

As indicated above, the circuits of an accumulator are divided into three groups for purposes of explanation. First, there are the program control circuits which comprise the circuits of the receiver and transceiver plug-in units, their associated switching circuits, and the repeater plug-in unit. Second, the common programming circuits connect by means of interconnection plugs (see, for example, the terminals marked ST 6, 7, and 8 on the left edge of PX-5-304) to the program control circuits. Third and last, there are the numerical circuits which extend from the input plugs $SV_1, \dots, SV_5$ through the decades and PM unit to the output plugs SW_1 and SW_2 (at the top of the block diagram). The common programming circuits directly control the numerical circuits by opening certain gates and in some cases introducing certain pulses into the numerical circuits. The following table summarizes the gates and pulses produced by the program control circuits and by the common programming circuits.

TABLE 4-1.

Program Control Circuits			Common Programming Circuits		
Switch settings			Gates provided at	Gates Provided	Pulses Provided
Operation Switch	Clear Switch	Repeat Switch			
α	0	—	SU 1	Carry gate to tubes 19 and 20 in the decades and α input gates opened.	None
β	C	—	SU 2	Carry gate as above and β input gates opened.	
			SU 10	Gates E49 and E50 opened.	<u>1</u> pulse added in first decade
A	0	1	SU 6	Gates H47 and J49 opened.	<u>Tens pulses</u> to cycle decades and <u>Nines pulses</u> for transmission over add output SW ₁
AS	0	—	SU 7	Gates G47, G49, H49, and M41 opened.	<u>Tens pulses</u> to cycle decades, <u>Nine pulses</u> for transmission over add output and subtract output, and <u>One-primed pulse</u> for transmission over SW ₂
S	0	—	SU 8	Gates F47, F49, and M42 opened.	<u>Tens pulses</u> to cycle decades, <u>Nines pulses</u> for transmission over subtract output, and <u>One-primed pulse</u> for transmission over SW ₂
A	C	—	SU 6	Same as for A above	Same as for A above
			SU 9	Opens M44 passing CCG to clear tubes in the PM-Clear unit.	

4.1. THE PROGRAM CONTROL CIRCUITS

4.1.1. General description of a non-repeat program control circuit

Suppose that a program pulse arrives over the input terminal 11 (lower left corner of PX-5-304). This positive pulse will cause one half of 66 (tube 66 is a 6SN7, a double triode tube) to become conducting. The drop in plate voltage will send a negative pulse into the flip-flop¹ causing it to be set. The indicated polarity of the output will then be reversed and half of 62 will go off (become non-conducting), causing the cathode follower¹ 63 to go on. The output of 63 comes from the cathode; therefore, when the tube becomes conducting the cathode potential rises with respect to that of the plate giving a positive gate voltage on the output. This output goes to deck 3 of the operation switch. If the operation switch is set at α , β , γ , δ , or ϵ this positive gate voltage appears on the interconnection terminals labeled SU 1 to 5. If the switch is set at A, Ag, or S then the gate appears on SU 6, 7, or 8. The fast output (cathode follower) is used there since these circuits must be set up before the 10 pulses arrive. The other output of the receiver flip-flop (which is positive after being set) opens the gate 61 (that is, allows a pulse on the first grid to cause the tube to conduct) and turns the buffer 62 on. This gives a negative voltage swing on the output which goes through the clear-correct switch and deck 2 of the operation switch. If the switch is set at α to ϵ , this signal appears on terminal SU 10 and will cause the correction to take place. If set at O, A, AS, or S the signal turns the inverter F50 off and the buffer (the other half of F50) on, giving a negative gate at SU 7 and will cause the accumulator to clear. After the gate 61 in the receiver is opened, the CPP (Central Program Pulse) arriving at the end of the addition time resets the flip-flop. The time constants are such that

1) For a detailed discussion of flip-flops, gate tubes, buffers, and inverters see Section 1.2.

gate 61 does not open in time to cause any conflict with the CPP which activates the receiver.

4.1.2. General description of a repeat program control circuit

Now, suppose a program pulse arrives at a transceiver, say at input terminal 5i. As in the receiver this pulse sets the flip-flop and within 15 μ s.¹ gives the positive gate through deck 3 of the operation switch to the interconnection terminals SU 1 to 5 or SU 6, 7, or 8. The other output (which is now positive) of the flip-flop turns the buffer tubes 61 on and opens the gate tube 62. If the clear switch is setting on clear, the negative gate output of tubes 61 goes through two decks of the operation switch and appears at SU 9 and at SU 10. The two tubes F50 are in the line from the receivers to raise the circuit to the d-c voltage level of outputs of the transceivers. The cross section of the receiver and transceiver (see PX-5-115) shows that the plate supply of the buffer 62 in the receiver is -345 whereas the plate supply of the buffer 61 in the transceiver is -235 volts. The negative gate from the right hand buffer 61 in the transceiver will turn the inverter J50 off giving a positive swing to one of the grids of the gate tube H50. The central program pulses (CPP) arriving at tube H50 will now be passed on into the repeater ring. (The CPP that stimulated the program control will not be passed). They go through the pulse standardizer (tubes 61, 62, and 63) and step the ring. If the repeat switch is set at 3 (as illustrated), then at the third addition time the ring will have stepped to stage three giving a positive gate through the repeat switch to the gate tube 62 in the transceiver. Note, that one repeater ring is used

1) This follows the practice that circuits are designed to operate in not more than half of the time which would suffice, for example, the 10 pulse gates (F-4, 47, connected to SU 6, 7, and 8) must be open inside of 32 μ s. (After CPP sets receiver or transceiver) in order to pass the first ten pulse. Actually, the time constant for these circuits depend upon the setting of the program switches. The maximum time constant occurs on a circuit when two accumulators are interconnected to form a twenty digit accumulator and all program switches are set to activate that circuit.

by all the repeat program controls. This causes the inverter 65 to go off opening the gate 68 and turning the buffers 63 on. The output from one of the buffers 63 goes through the clear switch and the operation switch giving a negative gate at $S_1 9$. The output of the other buffer 63 turns the tube J50 off opening the gate K50 (this process of opening gate K50 takes about 100 μs .) The JEP at the end of the third addition time passes this gate and turns the inverter K49 off (it over-rides the stepping pulse from H50) clearing the repeater ring back to stage one. The gate 68 being open, the central program pulse arrives at the end of the third addition time, resets the flip-flop and feeds through the transmitter (tubes 70, 71, and 72) giving a program output pulse which can be used to operate some other unit during the fourth addition time.

4.2. THE COMMON PROGRAMMING CIRCUITS

4.2.1. The receiving circuits.

The receiving circuits cause the accumulator to add to its present contents any ten digit signed number arriving through the input plugs SV_1 to SV_5 . This addition is accomplished by opening the proper set of receiving gates (L to A 41, L to A 42, ..., or L to A 45), and by providing for the carry-over between the various decades.

Suppose that an activated program control has its operation switch set on α . This applies a positive gate to $SU 1$. The interconnector cable carries this to ST_{11} . then it will cause tube C48 to become conducting and turn off the inverter J46. The positive gate from J46 opens the gate tubes L41 to A 41 and any digit or PM pulses arriving at the plug SV_1 will be transmitted into the corresponding decade or PM unit. Also, the positive gate from ST_{11} will open the gate tube E47 allowing the carry-clear gate (CCG) to be passed to the inverters A to D 49. The output from these inverters then opens the carry gates 19 and 20 in each decade. This carry-over will be explained in detail when the numerical circuits are taken up. (see Sec. 4.3.1.).

If the clear switch is set on C and the operation switch on a, then a negative gate will be applied to inverter G50 turning it off and opening the gates E49 and E50. This passes the 1' pulse through the interconnector terminals ST₂ 14 and 15 into the first decade of the accumulator. This provides for the correction of negative numbers where some of the last digits have been lost by the use of deleters (see Section 11.2.)

4.2.2. The add and subtract transmission circuits.

Suppose the operation switch of an activated program control is set at AS. Then a positive gate will appear at SU 7 and be transferred by the interconnector jumper to ST₁ 7. Then it will open the gate tubes G47, G49, H49, and M41. G47 will pass the cycling pulses (10 P) to the inverter H48 and the cathode follower L46. The output of L46 operates the buffers B, D, F, H, and K 46 resulting in the decades being cycled through all ten stages back to where they started. G49 will pass the 9 pulses to the inverter E 48 and the cathode follower D48. From there these pulses go to the gate tubes 22 in the decades and the gate tube 16 in the PM unit. Similarly, H49 will pass 9 pulses through C48 and F48 to the gates 21 and 15. M41 passes a 1' pulse through the transmitter (23, 24 and 25 in the PM unit) to the interconnection terminals SU₁ 17. From there it goes to the significant figure switch and into one of the output terminals of the subtract output SW₂.

If the operation switch is set at A then the cycling pulses (10P) are provided by gate H47 and the 9 pulses (9P) are supplied to the add gates 21 of the decades and 15 of the PM unit by the gate J49. If the switch is set at S then the cycling pulses are provided by F47 and 9 pulses are sent to the subtract gates 22 of the decades and 16 of the PM unit by gate F49; also, M42 provides the correction pulse (1'P). If the clear switch of the activated program control is set at C then at the end of the operation (one addition time in the case of receivers and one to nine addition times in the case of transceivers depending upon the setting of the repeat switch) a negative

gate voltage will appear at SU 9 and from ST₁ 9 it will turn off the inverter J50 opening the gate M45. This passes a carry-clear gate (CCG) to the clear tubes (1 to 10 in the PM-Clear unit).

4.2.3. General description of the clear circuits

For purposes of rounding off numbers the decades of an accumulator are provided with clear-to-five circuits. To the left of the PM unit is seen the significant figure switch. The setting of this switch determines which decade clears to 5. All other decades clear to zero. For example, to round off to three significant figures the seventh decade is cleared to five before the number to be rounded off is put in the accumulator.

Inspection of a decade plug-in unit on the cross-section PX-5-115 shows that clearing any stage in the ring is accomplished by a direct connection to the clear tubes (1 to 10 in the PM unit) labeled "clear T", and a return circuit labeled "clear R" which returns to a resistance. The block diagram shows that all stages except zero and five connect directly to the clear tubes and the resistance, whereas, stages zero and five connect to four decks of the significant figures switch. The significant figures switch effectively reverses the connections to the zero-five leads in one decade causing the decade to clear to five instead of to zero.

With the significant figures switch setting as illustrated, the ninth decade will clear to five, giving numbers with one significant figure. A clear signal coming from the clear tubes in the PM unit will go directly to the upper connections to stages 1, 2, 3, 4, 6, 7, 8, and 9 in all decades; through deck one of the significant figures switch, it will go to the upper connections to the fifth stages in all decades except the ninth (corresponding to one significant figure) and in the ninth through deck 2A it will go to the upper connection of the zero stage. The return circuits come back in a similar manner through decks 2 and 1A.

The clear signal arises by a carry-clear gate being passed by tube M44 to the inverter M43 and thence to tube 1 in the PM unit. If the accumulator is being used with the multiplier or divider the clear gate may be introduced directly into the PM unit as illustrated. The gate M44 will be opened to pass a carry-clear gate in the following cases.

a) If the ENIAC is initially cleared the initial clear gate (ICG) arrives through the buffer M45.

b) If the accumulator is set to selective clear and the selective clear gate (SCG) is provided at the initiating unit (see 2.3.1.) then the inverter J50 is turned off by the signal from the buffer M48.

c) Or, if the program control switch of an activated program circuit is set to O, A, AS, or S and the clear switch to C then at the end of the operation a negative gate appears at ST₁ 9 which turns off the inverter J50 and opens the gate M44.

The ICG also clears the repeater ring back to stage one by gating a CPP at K50.

4.2.4. A description of the interconnection features

The outputs of the program control circuits appear at terminals SU located on the front panels. Just above these are the terminals ST. It is expected that the usual plan will be to operate as a ten digit accumulator. In this case a jumper is plugged from the terminals SU₁ to ST₁ (PX-5-121) and a load box is placed in ST₂. This effectively connects together the interconnector terminals located next to each other on the block diagram PX-5-304. In case of twenty digit operation all the program controls must operate in parallel; this means that the load resistors for these circuits cannot be built in since what is correct for separate operation would not be correct when they are operating in parallel. Thus, the load resistors are on a unit which is plugged into the front panel. Only one such unit is used with each accumulator or with each pair of accumulators when con-

nected to form a twenty-digit accumulator.

If two accumulators are to be interconnected to form a twenty digit accumulator then the terminals SU_2 and ST_2 of the left hand accumulator are jumped respectively to SU_1 and ST_1 of the right hand, SU_1 of the left hand is jumped to ST_1 of the left hand, and a load box is placed in ST_2 of the right hand accumulator. This makes the carry-over from the tenth decade of the right hand accumulator go into the first decade of the left hand and the 1' pulse (correction pulse) go into the first decade of the right hand accumulator. The "10" output of the significant figure switch of the left hand accumulator goes to the input of the significant figure switch of the right hand accumulator. The "0" output of the right hand significant figure switch goes to the input of the units decade of the left hand accumulator.

A list of connections for ten and twenty digit operation are given in tables 4-2 and 4-3. Note that the PM unit of the right hand accumulator is not used in twenty digit operation.

4.3. NUMERICAL CIRCUITS

4.3.1. General description of a decade plug-in unit.

The pulse standardizer (tubes 11, 12, and 13) consists essentially of four triodes (11 being a double triode 6SN7). The output of tube 12 goes both to tube 13 and the gate 14. The output of 13 goes to the decade ring. In the block diagram the large numbers in the stages of the ring represent the positions of the tube while the small number just outside the respective stages represents the digit corresponding to that stage. After clearing, the ring is setting at zero (for a detailed discussion of the operation of ring counter circuits, see 1.2.2.).

Receiving Numbers. If five pulses arrive on the digit input they will pass through the pulse standardizer and step the ring up to position five. Pulses will also go to the gate tube 14 but will have no effect since the second grid of that tube is negative being connected to the negative output

TABLE 4-2

Vertical interconnector cable. (PX-5-121)
Just one used for either a 10 or 20 digit accumulator.

SU_1	ST_1	
1	1	These connections enable any program control circuit to cause the common programming circuits to make the accumulator receive on channels
2	2	
3	3	
4	4	
5	5	
6	6	These connections enable any program control circuit to cause the common programming circuits to make the accumulator transmit on A, AS, or S.
7	7	
8	8	
9	9	
10	10	This connection provides for the correction pulse.
11	11	
12	12	
13	13	This connection in the ST_1 end takes the carry of the 10th decade into the input of the PM unit.
14	14	
15	15	
16	16	
17	17	This connection takes the correction pulse transmitted by the transmitter (23-25) in the PM-Clear unit to the input of the significant figure switch.
18	18	

Terminal 18 is a ground connection in each case.

Note that the load box plugs into terminal ST_2 and has jumpers which connect terminals 14 and 15 and 16 and 17. This takes the correction pulse into the units decade input (units decade of right hand accumulator in case of twenty-digit operation) and the 16 to 17 connection takes the "10" output of the significant switch to the units channel of the subtract output.

TABLE 4-3

Horizontal interconnector cable. (PX-5-110).

<u>SU₁</u>	<u>ST₁</u>	
1 _____	1	These connections cause any program control to cause the two accumulators to act in unison when receiving on a to e .
2 _____	2	
3 _____	3	
4 _____	4	
5 _____	5	These connections cause the accumulators to act in unison when transmitting on A, AS, or S.
6 _____	6	
7 _____	7	
8 _____	8	
9 _____	9	This connection causes the clear circuits to act in unison.
10 _____	10	{ This connection allows any program control to provide the correction pulse at terminal ST ₂ ¹⁴ of either accumulator.
11 _____	11	
12 _____	12	
13 _____	13	
14 _____	14	
15 _____	15	{ For upper cable this connection takes the output of the 10th decade of right hand accumulator to 1st decade input of the left hand accumulator.
16 _____	16	
17 _____	17	{ This connection in upper cable takes "0" output of significant figure of right hand accumulator into the units channel of the subtract output of the left hand accumulator.
18 _____	18	{ This connection takes "10" output of the significant figure switch of the left hand accumulator to the input of the significant figure switch of the right hand accumulator.
		Terminal 18 is a ground connection in all cases.
		The connections 15, 16, and 17 serve no purpose in the lower interconnector cable (between terminals SU ₁ and SU ₂).

of the ninth stage of the decade ring. Suppose that six more pulses arrive. Four of these will step the ring up to position nine. The fifth will step the ring from nine to zero and will pass through the gate 14 setting the decade flip-flop and turning the inverter 15 off producing a positive pulse at gate 19. Since the incoming digits arrive before the carry gate goes on (see PX-9-301) this pulse does not pass gate 19. The sixth pulse steps the ring from zero to one. The carry gate comes on later in the addition time, opening gates 19 and 20. Since the flip-flop has been set the reset pulse RP (which arrives just after the carry gate comes on) is passed by gate 18 through the inverter 15 and through gate 20 to the digit input of the next decade to the left. This is called the delayed carry-over. Thus, six plus five is eleven.

Suppose that a decade registers nine and a carry-over arrives from the next decade to the right. This carry-over pulse besides stepping the ring from nine to zero also passes through gate 14 turning off the inverter 15. This gives a positive pulse to gate 19 and since the carry gate is still on, there is a carry-over to the next decade to the left. This is called the direct carry-over. If all decades register nine, one may have a sequence of nineteen such carry-overs in the case of a twenty-digit accumulator so the carry gate has been made sufficiently long to provide for this possibility.

Transmission of numbers. The above description of a decade unit has been in terms of receiving numbers. Now consider an activated program with the program switch set to AS, say. In this case the cycling pulses are arriving at the digit input, there is no carry over since the carry gates A to E 47 are not open, and the nine pulses (9P) are arriving at the gates 21 and 22 in the decade. As indicated in the diagram, normally (after initially clearing) gate 22 is open. Suppose the decade registers the digit three. What happens during the twenty pulse times of an addition time is

illustrated in the table 4-4. Note, that the tens pulses arrive $2 \frac{1}{2} \mu s$. after the nines pulses; this gives the decade ring $7 \frac{1}{2} \mu s$. in which to step and also $7 \frac{1}{2} \mu s$. for the flip-flop (16, 17) to be set. If the operation switch is set at A instead of AS the only difference is that the 9 pulses do not appear at gate 22 and the 1' P is not provided. In case the switch is set at S the 1' P is provided and the 9 P appear only at gate 22. If the clear switch is set to C then at pulse time 10 the carry-clear gate appears at gate tube H45 and the decades are cleared back to zero.

4.3.2. General description of a PM - Clear plug-in unit.

The PM-Clear unit contains a binary counter to register the sign (PM) of numbers. Since the binary counter is much simpler than the decade counter the pulse standardizer is also simpler. It contains three tubes in two envelopes (a 6SN7 for tube 11 and 12 is a 6V6). For a detailed discussion of PM counters see Tubes 1 to 10 are part of the clear circuits and have been described in section 4.2.3. Tubes 15 to 22 comprise the transmitter circuits which transmit the sign indication over the add and subtract outputs. Tubes 23 to 25 form a standard transmitter for the 1' pulse (used to give complements with respect to 10^n instead of $10^n - 1$, where n is the setting of the significant figures switch.)

An odd number of pulses arriving at the PM binary counter will change its resulting position. An even number of pulses will leave it the same as it was to start with. If the number registered by the accumulator is positive and an activated program control has its operation switch set to AS then nine pulses will pass gate 15. If the registered number is minus then nine pulses will be transmitted through gate 15 over the add output and none will go past gate 16.

Table 4-4

Pulse time	General pulses	Cycling pulses (2 1/2 p sec. late)	Decode Registers	Pulses trans. over SW ₂ (subtrct)	Pulses trans. over SW ₁ (add)
16			3		
17	CPP		3		
18			3		
19	RP		3		
0			3		
1		1st	4	1st	
2		2nd	5	2nd	
3		3rd	6	3rd	
4		4th	7	4th	
5		5th	8	5th	
6		6th	9	6th	
7		7th	0		1st
8		8th	1		2nd
9		9th	2		3rd
10		10th	3	1st if decode corresponds to 1st sig. figure	
11			3		
12			3		
13	RP		3		
14			3		
15			3		
16			3		

V. THE HIGH SPEED MULTIPLIER

The high speed multiplier is a unit of the ENIAC capable of forming the product of two ten digit numbers in thirteen addition times (0.0026 secs.). It is called a high speed multiplier because, by making use of multiplication tables, it is able to produce a product much more rapidly than if the method of repeated additions were used. In the method of repeated addition a maximum of nine addition times must be allowed for each digit of the multiplier giving a possible total of ninety addition times for a ten digit multiplier.

The method of multiplication used by the high speed multiplier is to multiply the entire multiplicand by each digit of the multiplier in turn and to sum the resulting products taking into account their proper decimal positions. Thus, only one addition time is required for each multiplier digit (plus three extra addition times for operations that must be performed for each multiplication).

The circuits are so arranged that the digit of the multiplier which is being used at a particular time excites a bus of two multiplication tables, a tens table and an units table. The product of two single digits is usually a two digit number; thus, the output of the tens table is the tens digit of the products of the multiplier digit and the digits one to nine inclusive, while the output of the units table is the units digit of the products of the multiplier digit and the digits one to nine inclusive. The use of the two tables makes it possible for the partial products to be received simultaneously into two accumulators without interference.

Since the product of two ten digit numbers is usually a twenty digit number it will be necessary to use two accumulators interconnected to form a twenty digit accumulator to receive the right hand (units) partial

products and similarly for the left hand (tens) partial products. Thus, for ten digit multiplication the high speed multiplier will work in conjunction with six accumulators, one for the multiplier, one for the multiplicand, two for the left hand partial products, and two for the right hand partial products.

Throughout most of the discussion of this chapter it will be assumed that accumulators 9 and 10 are used for the multiplier and multiplicand, respectively, that accumulators 11 and 12 (connected to form a twenty digit accumulator) receive the left hand products, and that accumulators 13 and 14 (also used as a twenty digit accumulator) receives the right hand products. The setting of the respective program controls on these last (two twenty digit) accumulators determines whether the final product appears in 11 and 12 or 13 and 14.

After the multiplying operation has been carried out for each digit of the multiplier (certain complement corrections may be needed) the right and left hand products are collected into one accumulator. In the fourteenth addition time (for a ten digit multiplication) the product may be transmitted to some other unit and simultaneously the multiplier and multiplicand accumulators may receive the next numbers to be multiplied.

5.0. INTRODUCTION. This description of the multiplier will be given in terms of the block diagram PX-6-308 and the cross section diagrams PX-6-112 and PX-6-112A. In the upper left corner of the block diagram is seen the multiplier selector. To the right of this (upper center) is the tens multiplication table and in the upper right corner is the units multiplication table. Below the tables are the table gates which pass the 1, 2, 2', and 4 pulses. Below the gates are the two multiplicand selectors, one for the tens table and one for the units table. The output of the multiplicand selectors goes to the shifters and thence to the digit outputs.

These circuits comprise what will be called the numerical circuits.

To control the operation of these numerical circuits there are the common programming circuits. The common programming circuits consist of the multiplier ring (located on the block diagram under the multiplier selector), the round-off circuits (A' 46 to 49, A" to H" 45, and K" 45), the complement correction circuits (B" 46 to 50, C" 46 to 50, and L" 43 to 47), the receiving circuits (H, J, and L 41 to 50), the product disposal circuits (D" to J" 46 to 50), the clear circuits (A to L 11), reset circuits (to the right of the ring), and below the reset circuits a receiver to cause the product accumulators to receive the partial products and a circuit (A" 47 to 50) to cause the collection of the right and left hand products.

There remains the program control circuits. These consist of twenty four transceivers, their associated switches and buffer tubes. Associated with each transceiver we have the following switches: a) places switch, b) multiplier and multiplicand clear switches, c) significant figures switch, d) multiplier receive switch, e) multiplicand receive switch, and f) the product disposal switch.

The program control circuits, the common programming circuits, and the numerical circuits will be described in detail in the next three sections. The fourth section will be devoted to examples.

5.1. PROGRAM CONTROL CIRCUITS.

5.1.1. The buffer plug-in units. As shown in the block diagram there are two buffers on the program input lines to each transceiver. There are eight transceivers located on each of the three panels of the multiplier. The sixteen buffers for each panel are located on two plug-in units. The tubes in these plug-in units are numbered from 61 to 68. Note that tubes 61 and 62 are associated with the first program circuit. Those numbered

63 and 64 would be associated with the second program circuit and so forth. This buffer system means that at most five program controls need be used in each of the multiplier and the multiplicand accumulators in order to receive the multipliers and multiplicands for all possible multiplications.

A program pulse arriving on terminal 1i, for example, would turn the buffers 61 and 62 on giving a negative pulse at the receive switches (see 5.2.3). Depending upon the setting of these switches pulses may be obtained out of one of the terminals R_A to R_E and one of D_A to D_E .

5.1.2. Transceivers. These transceivers are standard, that is, they are identical with the transceivers used in the accumulators, the function tables, the divider, and the constant transmitter. This simplifies the problem of maintaining operation, since, if any one fails the unit can be pulled out and a spare put in.

5.1.3. Program control switches. With each transceiver there are the following switches:

a) Places switch. This switch determines how many digits of the multiplier are used in the multiplication. Since the time required for a multiplication is $n+3$ where n is the number of digits in the multiplier the time required for a problem can be materially shortened if fewer than ten digits of the multiplier can be used. With the place switch setting at 8 (as illustrated) the multiplier ring will step to stage 10 using eight digits of the multiplier. The inverters G' 45 and H' 45 being off the gate H' 46 will turn the inverter F' 47 off and on the next addition time a CPP will pass gate F' 48 and through the inverters G' 47 and D' 47 will clear the ring to stage 13.

b) Multiplier and Multiplicand clear switches. Depending upon

the setting of these switches the following four possibilities arise:

	Multiplier Clear Switch	Accumulator Clear Switch	Result
(1)	O	O	Neither multiplier or accumulator clear.
(2)	C	O	An activated program causes inverter J 30 to go off opening the gate H 30. This gate passes the CCG to the inverter G 31 which turns the buffer J 29 on. The output of J 29 goes directly to the clear tubes 2 to 10 in the PM unit of the multiplier accumulator.
(3)	O	C	In this case A 31 goes off opening the gate B 31. The CCG turns off the inverter C 30 which in turn causes the buffer H 29 to conduct. The output of H 29 goes directly to the clear tubes of the multiplier accumulator.
(4)	C	C	Here the inverter E 30 goes off opening the gates D 30 and F 30. As above, the clear gate is passed into the two sets of clear tubes in the respective PM units.

c) Significant figures switch. Depending upon the setting of the significant figures switch a 5 is put into one of the decades of the left hand product accumulators. If the switch is setting on 2 (as illustrated) at the second addition time the digit 5 will be passed by gate H" 45 into decade number 8 of product accumulator number 11 (corresponding to digit output terminal SV₄).

d) Multiplier receive switch. This switch determines whether the multiplier accumulator receives the multiplier on the input terminals a, b, c, d, e, or f. The program pulse arriving over li, for example, turns the buffer 61 on giving a negative pulse through the switch turning inverter H 46 off (if the switch is setting as illustrated). This causes the buffer H 46 (these are the two triodes of a-6SN7) to conduct and the transmitter J to L 46 gives a program pulse out of the terminal R₆ located

on the front of panel one. This will normally be connected to the input of a receiver or a transceiver located in the multiplier accumulator and the corresponding program switch will be set to receive on ϵ .

e) Multiplieand receive switch. This switch operates in a manner entirely analogous to the multiplier switch described above.

f) Product disposal switch. Suppose that the product is finally collected in accumulators 13 and 14. The setting of the product switch determines what the pair of accumulators (operating as a twenty digit accumulator) do with the numbers. Suppose the disposal switch is setting on SC (as illustrated). The program which started the multiplication set the flip-flop (66, 67 in transceiver) and so opened the gate 62 in the transceiver. At the end of the multiplication the reset signal arrives, passes gate 62 and turns off the inverter 65. This turns on the buffer 63 giving a negative gate through the disposal switch turning off inverter E" 46 opening gate E" 47. At the beginning of the next addition time a CPP is passed through the transmitter E" 48 to 50 to the terminal SC on front panel number three. Generally, the operator will connect this output to the input of a program control circuit on accumulators 13 or 14, say, and the corresponding program switch will be set to S and the clear switch to C. If needed, the other outputs A, S, AS, AC, and ASC, can be connected to the inputs of program control circuits on accumulators 13 and 14 (or 11 and 12 if the product is collected here) and the corresponding switches set accordingly.

5.2. COMMON PROGRAMMING CIRCUITS.

5.2.1. The multiplier ring. This is a fourteen stage ring which controls the timing of the multiplication process. Whenever a program control circuit is activated the inverter H' 44 goes off opening the gate F' 44. This gate then passes central program pulses through the pulse standardizer E' to B' 44 to step the ring. Whenever the ring is not at stage one the gate J' 44 is open. This passes central program pulses to the inverter H' 44 and thence to the gate G' 44. If the initial clear gate is on the CPP pass G' 44 and step the ring until it arrives at stage one.. When

it reaches stage one J' 44 closes shutting off the CPP.

This method of initial clearing by stepping the ring to stage one is used here since, as described below, the regular clearing circuits operate in conjunction with the places switch to clear the ring to stage 13 in the process of terminating the multiplication.

Suppose that program control 1 has been activated. The multiplier ring steps (at the end of the next addition time) to stage two turning A' 45 on and the inverter B' 45 off. This opens the gates A' 46 and 47 which pass the 4 pulses and the 1' pulse to give a five in some decade of accumulators 3 or 4. The output of B' 45 also goes to gate B' 47 which gates a 1 pulse. This 1 pulse turns the inverter B' 48 off and thence sets the two receivers. The outputs of these two receivers come to front of panel three. (See PX-6-304). From there these gate signals will be taken by special interconnecting jumpers to interconnector terminals ST₁ 1 on accumulators 11 and 12 and accumulators 13 and 14. Inspection of the accumulator block diagram PX-5-304 shows that this will cause the product accumulators to receive the partial products over the input digit terminals a . This is an example of a receiver located in one unit operating the governing circuits of another unit.

The timing is important here:

Pulse time	17	18	19	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	CPP steps		1 P sets						4 P				1' P							
	ring to		receivers						start				arrives							
	second		to cause																	
	stage		partial prods.																	
			to be received																	

Thus, in one addition time the ring steps to the second stage, the product accumulators are set to receive, and the five pulses for the round-off are put into the proper decade. The CPP that steps the ring could not be used to operate the receivers because of the time it takes for B' 47

to open.

The next addition time the ring steps to stage three. B' 42 goes on and inverter L 1 off opening the gates for the tenth digit of the multiplier (gates K 2 to K 11). Depending upon the tenth digit of the multiplier one of the lines through the multiplication tables will carry a negative gate (which will turn off certain pulse gates). At the same time inverter B' 41 will go off causing the bottom row of gates in the two shifters to open. Thus, the tens partial product will feed into accumulator 11 and the units partial product into decades 1 to 9 of accumulator 13 and decade 10 of accumulator 14. Notice that the units product is already shifted one place to the right. Thus, when the right and left hand products are collected at the end of the multiplication no extra shifting will have to be done.

As the ring steps from 3 toward stage 12 the gates for successive digits of the multiplier are opened and the gates on corresponding levels in the shifters are opened.

If the place switch is setting on 8 the inverter G' 45 is off opening gate H' 46. When the ring reaches stage 10 the inverter H' 45 goes off causing the gate H' 46 to go on and the inverter F' 47 to go off. This opens the gate F' 48 and at the end (pulse time 17) of the addition time a CPP turns the inverters C' 47 and D' 47 off clearing the ring to stage 13 (this clear signal overrides the stepping signal which would normally step the ring to stage 11). The output of F' 47 also gates a CPP at the end of the addition time at E' 48 which turns the inverter F' 49 off causing the receiver flip-flops to reset. This causes the product accumulators to stop receiving the partial products. The output of F' 47 also opens the gates B" 46 and L" 47. The CPP gated by B" 46 ultimately gives a program pulse out RS if the multiplier is negative and out DS if the multiplicand is negative. If both multiplier

and multiplicand are negative $L'' 47$ gates a 1st pulse which finally goes into the FM channel to accumulator 13.

When the ring steps to stage 13 the inverter $L' 45$ goes off and gates $D 49$, $K'' 50$, and $A'' 47$ are opened. At the 14th addition time $D 49$ gates a CPP which sets a flipflop causing programs 1 to 8 to reset. At the same time $K'' 50$ likewise causes programs 17 to 24 to be reset. $A'' 47$ gates a CPP during the 14th addition time which will generally be used to collect the right and left hand products. This pulse is transmitted to terminal F on the front panel. From there it will be jumped by the operator to a program tray and then used to program transmission of the left hand partial product, say, and the reception of this left hand product by accumulators 13 and 14.

Stage 14 of the ring causes programs 9 to 16 to be reset. The ring is located on panel two of the multiplier, so the gates 62 in transceivers 9 to 16 can be operated directly by the output of the ring. Since transceivers 1 to 8 are on panel one a special flip-flop (E and $F 49$) set by a CPP during the 13th addition time (passed by gate $D 49$ which is opened by stage 13 of the ring) provides the reset signal. Similarly, another flipflop (L'' and $K'' 49$) resets programs 17 to 24.

From stage 14 the ring steps back to stage 1 and stops. At this time the transceiver gives an output program pulse.

5.3. INITIAL CLEARING.

The initial clear gate is applied to the multiplier only through gate $B' 44$. This gate is open only when the program ring is not on stage 14. Thus, the effect of applying the initial clear is to cause the program ring to step around to stage one and stop.

In the case of the multiplier program ring the standard method of clearing is used for another purpose. Since the number of places of the multiplier that is used will vary from program to program a coincidence

between the setting of the places switch of an activated program and the stage on which the ring is setting will open gate F'48 causing the ring to "clear" to stage 13.

As with the accumulators there is no need to initially clear the transceivers. Any program pulses which get started in the programming circuits are allowed to run through the sequence (all sequences are broken at the master programmer, see 10.5), and then the decades of various units are cleared.

5.4. NUMERICAL CIRCUITS.

5.4.1 The multiplier selector. The multiplier selector is an array of one hundred gate or coincidence tubes. There is a tube for each possible digit in each place of the number. When the multiplier ring is at stage three the gates for the tenth digit of the multiplier will be open. If the first digit of the multiplier is 4, for example, then the static output of that stage of the tenth decade of the multiplier accumulator will be energized and the tube K 7 will conduct giving a negative gate to the inverter L 7. When this inverter goes off the tubes L 26 and K 26 go on giving a negative gate on line 4 into the multiplication tables.

5.4.2. The tables and the table gates. The 1, 2, 2', and 4 pulses come from the cycling unit trunk to buffers D 45 and 47 and E and F 48. From the buffers each pulse goes to an inverter and then to the table gates. Inspection of the cross section PX-6-112(k) shows that the table network is such that normally the second grids on the table gates are sufficiently positive that they pass the 1, 2, 2', and 4 pulses. Thus, the multiplication table is a so called "complementary" table, that is, all the gate tubes normally pass the 1, 2, 2' and 4 pulses and are turned off by the table if they are not wanted.

The digits of the multiplier are represented by the horizontal

lines through the table. The digits of the multiplicand are represented by the vertical groups of lines as labeled at the top of the table. In multiplying one times nine (consider one as the multiplier) the lines of the first column of the units table have no connections to the horizontal line 1. This allows gates D to G 21 to pass nine pulses which is the units part of the product of nine and one. In the tens table for the same two numbers there are connections to all four vertical lines. This means that gates D to G 41 will be closed, which is correct since the tens part of the product of 1 and 9 is 0.

Now, consider six times seven. On the horizontal line for six in the units table in the column for seven there are connections to 1, 2', and 4 but none to the 2 lines. This means that gate F 23 will be open and will pass two pulses but D, E, and G 23 will be closed. In the corresponding place in the tens table there are connections to the lines for 1 and 2. Therefore, the gates E and G 43 will be closed while D 43 will be open and will pass 4 pulses. Notice that zero in the multiplier must be connected to all vertical lines in the table so as to stop all pulses from going to the multiplicand selector. Also, note that zero gates are not needed in the multiplicand selector.

5.4.3. The multiplicand selectors. The output of the table gates for the nine column in the tens table goes to the top row of gates in the left hand multiplicand selector. The output of the eight column goes to the second row, and so forth. There is no need for a units column or a units row in the tens selector since one times any digit gives zero in the tens place. Similarly, in the units table the output of the nines column goes to the top row of the selector, et cetera.

Suppose the digits of the multiplicand are 98765 43210 and the multiplier digit is six. In the tens selector gates L' 21, K' 22, J' 23, ..., D' 28 will be open and will respectively pass 5, 4, 4, 3, 3, 2, 1, 1

pulses. In the units selector gates L' 1, K' 2, J' 3, ..., C' 9 will be open and will respectively pass 4, 8, 2, 6, 0, 4, 8, 2, 6 pulses. These pulses will feed through a inverter-buffer-inverter sequence into the shifter. If the six was in the third place of the multiplier then the gates H" 30 to H" 21 and H" 10 to H" 1 will be open in the respective shifters. Thus, the partial products of this step in the multiplication will arrive in the product accumulators in the following manner:

Acc. 11	Acc. 12	Acc. 13	Acc. 14
00000 00544	33211 00000	00000 00048	26048 26000

The output of the shifter passes through the driver tubes (A" to K" 44, for example). This is quite different from the standard transmitters used on the output of an accumulator (see PX-5-304).. This means that for reliable operation the product accumulators should be close to the multiplier and a short tray with no load box used to carry the partial products to the accumulators.

With the interconnector cables in use at the present time the partial products are received over the α inputs to the accumulators. Since the capacity on the outputs of the driver tubes mentioned above is limited (for the capacity limits here see the operators manual), the α inputs to the accumulators used to receive the partial products must not be used for any other purpose.

Note that rows of shifter gates are opened only when the program ring is on stages 3 to 12. Thus, when not multiplying (program ring is at stage 1) pulses (passed by the table gates and the multiplicand selector) are not passed by the shifter gates.

5.5. EXAMPLE.

Operation of multiplier.

Addition and
pulse time

Description

- 0.17 Program pulse arrives at transceiver.
This pulse passes buffers (61 and 62, for example) and depending upon the setting of the multiplier and multiplicand receive switches may be transmitted again. Gates F'44, K'46 and K" 45 (assuming the places switch is at 10 and that the significant figure switch is at 10) are opened.
- 1.17 A CPP passes F'44 to step the program ring to stage 2. Gates A' 46 and 47 are opened, as is gate B'47.
- 2.1 One pulse passes gate B'47 to set the l and r receivers.
2.6 Four pulses and a one primed pulse pass gates A' 46 and 47
to give five pulses out channel 10 of SV₃
- 2.10 The program ring steps to stage 3.
2.17 The output of stage three causes the multiplication of the multiplicand by the first digit of the multiplier to take place.
- 3.17 The program ring steps to stage 4 and multiplication by the second digit takes place.
- 4.17 The program ring steps to stage five, and so forth.
-
- 11.17 The program ring steps to stage 12, opening gate F'48, E'48, B"46 and L"47.
Multiplication by the tenth digit of the multiplier takes place.
- 12.10 1'P passes L"47 and (if both multiplier and multiplicand are negative) will be transmitted into the PM unit of accumulator 13.
- 12.17 A CPP passes F'48 clearing the ring to stage 13 opening gates D49, K"50, and A"47. A CPP passes E'48 to reset the l and r receivers. A CPP passes gate B"46 and may pass B"47 and/or C"47 to cause the complement corrections.
- 13.17 The program ring steps to stage 14. CPP pass gates D49 and K"50 to set the flip-flops E, F49 and K", L"49. A CPP passes gate A"47 to be transmitted to program the product collection (this pulse appears at terminal F).
- 14.10 The CCG may pass one or two of the gates B,D,F, or H 30 to cause the multiplicand and/or the multiplier accumulator to clear.

14.17

CPP pass gate 68 in the activated transceiver to reset it and to give an output program pulse. A CPP may pass one of the gates D" to J" 47 to program the product disposal. The program ring steps back to stage 1.

VI. DIVIDER AND SQUARE-ROOTER

The divider and square-rooter performs the operations of dividing and square-rooting ten and twenty digit numbers. To carry out these operations with ten and twenty digit numbers it makes use of four and seven accumulators, respectively. Thus, the divider and square-rooter unit itself is essentially a programming circuit which controls the operation of the associated accumulators.

The process of division is that of repeated subtraction. Thus, the numerator is in one accumulator and the denominator in another. The denominator is subtracted until an overdraft occurs. At this time the numerator is shifted (by transmitting to a shift accumulator and transmitting back with a shifter in the digit line). Note that the overdraft was not corrected as in some methods of division used on computing machines. Instead, signs are changed and the denominator is alternately subtracted and added between the shifts. The quotient is built up by the divider sending +1 or -1 into the proper decade of the quotient accumulator for each subtraction.

The process of square rooting is likewise accomplished by repeated subtractions (the quantity subtracted being increased by two each time in the proper decade). The number to be square rooted is placed in the numerator accumulator and the numbers to be subtracted are built up in the denominator accumulator. When an overdraft occurs the number in the numerator accumulator is shifted (similar to the shift in dividing) and certain corrections are made to the number in the denominator accumulator and the subtraction process is repeated. As the process continues twice the square root is built up in the denominator accumulator.

6.0. INTRODUCTION

Description of the divider will be given in terms of the block diagram PX-10-304. For purposes of description the circuits of the divider square-rooter will be divided as follows:

1) Program controls. The program control circuits consist of eight transceivers and their associated switches. These switches and their purposes are as follows:

a) Numerator receive switch. During the first addition time of the division this switch may be used to cause the numerator accumulator to receive either α or β .

b) Denominator receive switch. During the first addition time of the division this switch may be used to cause denominator accumulator to receive on α or β .

c) Numerator ^{clear} switch. At the end of the division or root process this switch may be used to cause the numerator accumulator to clear.

d) Denominator clear switch. At the end of the process this may be used to cause the denominator accumulator to clear.

e) Interlock switch. This switch decides whether or not the interlock feature is used. Suppose this switch is setting on HI. At the end of the division or root process the various flip-flops and rings in the divider square-rooter are cleared and an output program pulse is transmitted. If this switch is on I then this clearing process and output pulse does not occur until both a signal is received on one of the interlock inputs, (upper left corner of PX-10-304), and the division or root process is completed.

f) Answer disposal switch. This switch is connected to four receivers and thus gives four possible ways of disposing of the answer (that is,

four ways it could be transmitted).

g) Round-off switch. This switch decides whether the answer to the division or the square rooting process be rounded off.

h) Division-Square root and place switch. This switch determines whether the process is division or square rooting and how many places are used. There is a choice of 4, 7, 8, 9, or 10 places.

2) The common programming circuits. In the divider-square rooter (as in other units) the common programming circuits comprise all of the circuits except the program controls (described above) and the numerical circuits (described just below).

3) Numerical circuits. The numerical circuits of the divider-square rooter comprise the place ring and its associated gates (lower right hand corner of PX-10-304), the pulse gates (just above and to the right of the place ring), and the "1", "-1", "2", and "-2" receivers which open these gates.

6.1. PROGRAM CONTROLS

There are eight standard transceivers to receive the incoming program pulses. As in the case of the multiplier the incoming program pulse is immediately retransmitted to cause the numerator and denominator accumulators to receive their numbers without the loss of time. This retransmission takes place through buffers located on a separate plug-in unit (there are two such plug-in units altogether). Two such buffers, 67 and 68, are illustrated in the lower left corner of PX-10-304.

6.1.1. Numerator and denominator receive switches

The buffers 67 and 68 (described above) feed two switches located on the front panel, namely, the numerator and denominator receive switches. Each

of these switches have three settings, α , β and 0. The four outputs of these two switches go through inverters (B4, B5, A4, and A5) to four receivers (located on two plug-in units). The outputs of these receivers come to output sockets located on the front panel. The outputs may be connected directly to the common programming circuits of the respective accumulators by use of a special interconnector cable (See section 11.6.4.).

6.1.2. The numerator and denominator clear switches

The output of one of the buffers 63 (in the transceiver) goes to the numerator and denominator clear switches. This buffer 63 goes on only at the end of the division or rooting process (and possibly after an interlock signal) when clearing is taking place. The output of the switches (three outputs: numerator, denominator, or both) goes to inverters C49 and D49 and thence to gates A48, A49, B48, and B49. These gates pass the carry clear gate (CCG) through the inverters A47 and/or B47 and buffers A46 and/or B46. This signal goes directly to the clear tubes in the PM-Clear units of the corresponding accumulators (see PX-5-507). The following table illustrates what happens with the various settings of these switches:

TABLE 6-1

Nun. Clear Switch	Denom. Clear Switch	Effect (as tube 63 in transceiver goes on)
0	0	None
C	0	D49 goes off and gate B48 passes a CCG through the inverter B47 and buffer B46 to the clear tubes in the numerator accumulator.
0	C	Half of C49 goes off and gate A49 passes a CCG through A47 and A46 to the clear tubes of the denominator accumulator.
C	C	The other half of C49 goes off and gates A48 and B49 pass CCG's through A47 and A46 in one case and B47 and B46 in the other.

6.1.3. Interlock Switch

The setting of this switch determines whether the interlock feature is used or not. If this switch is setting at "NI" the buffer 61 (in the transceiver) causes the inverter L49 to go off and the gate K49 to open. The CPP's passed here turn the inverter H49 off. The gate H50 is opened at the end of the division or square rooting process and the CPP's from H49 are passed to provide the clearing action.

If the interlock switch is setting at "I" the other half of L49 is turned off and L48 is open. In order for a CPP to get through to gate H50 the flip-flop H, J 48 must be set opening gate J49. This flip-flop is set only when a signal arrives over one of the interlock inputs turning on one of the buffers F 46 to 48 or G48. (This pulse may arrive during the division or root process or even before it starts).

Thus, if the switch is set on "I" the clearing signals and the output program pulse are not provided until; (1) the division or square rooting process is completed and the control ring steps down to stage seven, and (2) a program signal has arrived over one of the interlock input terminals and set the flip-flop H, J48. Note that the interlock flip-flop H, J48 is not reset unless the program control being used is set to "I". This means that a number of divisions or square roots may be done and then the interlock feature be used at the end even though the interlock pulse arrived during one of the earlier divisions.

6.1.4. Answer disposal switch

This switch has five positions, four of these go respectively to four receivers and the fifth is an "off" position. At the end of the division or square rooting process (and after the interlock signal has arrived if the interlock switch is at "I") the buffer 63 (in the transceiver) goes on. This

may (depending upon the setting of the switch) cause one of the inverters E46 or E47 to go off opening one of the gates C or D 46 or 47. The CPP passed by one of these gates will turn the corresponding inverter C or D 48 or 49 off activating the corresponding receiver. The outputs of this receiver go directly (provided the operator connects them) to the common programming circuits of the quotient accumulator or to the denominator accumulator depending on the interconnector cable used (see section 11.6.4.) The timing of the operation of these circuits is explained in sections 6.4.1 and 6.4.2.

6.1.5. Round-off Switch

The round-off switch is a double-pole, double-throw switch which determines whether the answer is to be rounded off or not. One pole of the switch operates in case of division and the other in case of square rooting and works in conjunction with one deck of the root-divide and place switch. The four terminals connect to four inverters (the four triodes of L4 and L5) which in turn connect to the gates L3, K3, K4, K5, K6, and L6. These gates provide the division pulse (DP), the square root pulse (SRP), and the round-off pulse (ROP).

6.1.6. Root-Divide and Place Switch

Of the two decks of this switch one (the one on the right on PX-10-304) determines whether the process is to be division or square rooting. This deck takes the output of buffer 61 in the transceiver to the round-off switch described above. The other deck determines how many places the answer is to contain. This switch handles two jobs. This means that the number of places used in a division or a square rooting is restricted to 4, 7, 8, 9, or 10.

6.2. THE COMMON PROGRAMMING CIRCUITS

The common programming circuits, which constitute most of the divider, will be divided into sections as indicated below. This subdivision is a logical one, that is division is with respect to the purpose of the particular circuit and not with respect to physical location. To a considerable extent this division is indicated on the block diagram PX-10-304 by the spacing between circuits. The subdivisions are:

- a) The pulse source circuit. This circuit centers around the pulse source flip-flop E 4 and 5 located to the right of the program control circuits on the block diagram. The circuit extends up to and including the gates L3, K3 to L6, and L6.
- b) The program ring circuits. The program ring is located on the upper left portion of the block diagram. This circuit includes the program ring flip-flop A, B 6 and the associated gates.
- c) The sign indication circuit. This circuit (located in the upper right hand corner of the block diagram) includes the denominator flip-flop, the numerator ring, and the sign indicating matrix (just below).
- d) The over-draft circuit. This circuit determines when the numerator changes sign, that is, when there has been an overdraft. This circuit is located at the top center of the block diagram.
- e) The add-subtract circuit. This circuit programs the trial additions or subtractions and is located directly under the numerator ring and the sign indication circuit. Its left hand part consists of the N_a receiver and the D_y and Q_y receivers. The right hand part consists of the D_S and D_A receivers and the associated gates, inverters, and buffers.

f) The round-off circuit. The round-off circuit is located practically in the midst of the add-subtract circuits. It consists of the round-off flip-flop L 11 and 12 and the associated gates and inverters. It includes the gates G8, H8, E13, and F13.

g) The root correction circuit. This circuit is essentially the receiver D_y and the root reset lines.

h) The shift circuit. The shift circuit is below the overdraft circuit and to the right of the pulse source circuit. At the time of over-draft it causes the number in the numerator accumulator to be transmitted to the shift accumulator and then to be transmitted back again. A shifter is used on the input (a) to the numerator accumulator so that the number is shifted one place to the left when it comes back from the shift accumulator. The shift circuits comprise the S_a , N_A , S_A , and N_a receivers and their associated gates and inverters.

i) The clear and interlock circuits. The clear circuits are located in the upper left hand corner of PX-10-304 to the left of the program ring. These circuits determine when the division or rooting process has finished and (depending upon the setting of the interlock switch of an activated program control) perhaps when some other sequence of computations is finished (as indicated by the output program pulse of that sequence arriving over one of the interlock inputs). Since a division or root process is of unknown length this allows the operator to carry on other computations simultaneously and then to follow with another sequence of computations only when both the division or root process and the other sequence are completed.

6.2.1. The pulse source circuits.

The pulse source flip-flop is normally in a state which causes gates

F4 and F6 to be open. The flip-flop is in this position except for period III (see PX-10-305 or PX-10-306, the division and square rooting time tables). Thus, during periods I, II, and IV central program pulses pass gate F4, go through the inverter G4 and the cathode followers G3 and H4. This produces a general pulse (GP) which does the following things

- (1) goes to gates K6 and L6 to produce a division pulse (DP),
- (2) goes to gates L3 and K3 to produce a square root pulse (SRP),
- (3) goes to gate A7 to clear the program ring,
- (4) goes to gate B7 to set the program ring flip-flop,
- (5) goes to gate D9 to produce a "P" pulse which causes an add-subtract cycle to take place (see the time tables PX-10-305 and PX-10-306),
- (6) goes to gate E9 to cause a shift cycle to take place,
- (7) goes to gate C11 to produce a root reset pulse,
- (8) goes to gate C9 to produce a "P" pulse which starts another add-subtract cycle after a shift cycle is completed, and
- (9) goes to gate D6 (top of drawing) to step the numerator ring and set the denominator flip-flop in case of negative signs.

The gate F6 passes the one-primed pulse and during a shift cycle this pulse passes gate L45 to step the quotient place ring. Using the 1'P here allows extra time for the quotient ring to step and set up its array of gates.

During period III the flip-flop E 4, 5 is set. This opens the gate F5 and the central program pulses pass the inverter G5 and the cathode follower A12 to produce a third period pulse (IIIP). This third period pulse does the following things:

- (1) goes through the buffer C12 and the inverter D13 to give a root reset pulse,
- (2) goes to the gates K4 and K5 to produce a round-off pulse (ROP),
- (3) goes through the buffer and inverter A12 and the buffer A13 to the pulse standardizer of the program ring.

The pulse source flip-flop is set during a shift sequence by a pulse passing gate E6. This gate will be opened by the inverter D50 going off, and this is caused by a coincidence between the setting of the place switch and the position of the quotient place ring as detected by one of the gates A to C 41, 42, or 43. This flip-flop is reset either by the program ring reaching stage seven and opening gate F3 to pass a CPP or by a C1' pulse arriving at the buffer F3 from the clear circuits. The C1' pulse resets this flip-flop when initially clearing whereas the CPP passing E3 indicates the division or rooting is completed and by resetting E4, 5 prevents the program ring from stepping until A, B, C is reset and another program control is activated.

6.2.2. The program ring circuits.

Normally (after initially clearing) the program ring flip-flop (A, B 6) causes the gates A10 and A11 to be open. Thus, as the process of division or square rooting starts the DP pulses or the SRP pulses pass one of these gates and (going through the inverter A12 and buffer A13 to the pulse standardizer) step the program ring. In two addition times (see section 6.4.1.) the program ring will step to stage one. The output of this stage opens gates A7 and B7. A7 passes a general pulse (GP) which turns off the inverter A9 clearing (the clear signal overrides any stepping signal) the program ring back to stage one. At the same time a GP passes gate B7 to set the program ring flip-flop (A, B 6). This closes the gates A10 and A11 preventing the division pulses (DP) or the

square rooting pulses (SRP) from stepping the program ring again. After this the program ring remains in stage one until the third period pulse (IIIP) is produced. The IIIP will then cause the ring to step through all nine positions.

The positions of the program ring at all times is listed in the division and square rooting times tables PX-10-305 and PX-10-306. The following table gives the effect of each position of the program ring.

TABLE 6-2a

Period I		
Position of program ring	Division	Square rooting
A		
B	Gate D6 is opened to pass a general pulse (GP) through the inverter D5 to the gates K1 and B1 to set the numerator binary ring and the denominator flip-flop in case of negative signs.	Same as for division.
1	(1) Opens gates A7 and B7 to clear program ring and to set the program ring flip-flop. This causes the ring to clear to zero and remain there until period III. (2) Opens gate B8 which passes a division pulse (giving a P pulse) starting the first add or subtract cycle (IX).	(1) Same as for division. (2) Opens gates K8 and G7. These pass square rooting pulses (SRP) which cause +1 to be placed in the denominator accumulator to start the square root process.

TABLE 6-2a (Cont'd.)

Position of program ring	Period III (Operation is same in division or square rooting)
A	
B	Opens gate C8 to pass a round-off pulse (ROP) giving a P pulse which starts the add or subtract process. Gate D6 is opened but with no effect since general pulses (GP) are not produced in this period.
1	No effect since GP, DP, or SRP pulses are not produced this period.
2	
3	
4	
5	Opens gate D4 to pass an ROP giving a reset pulse which terminates the add or subtract process started above.
6	Opens gate J13 passing an ROP through the inverter K13 to gate K12. In case of no over-draft K12 passes this pulse through the inverter K11 into the round-off circuits.
7	Opens L 50 which passes a CPP to the clear circuits and opens E3 resetting the pulse source flip-flop.

6.2.3. The Sign Indication Circuit

In division this circuit (which consists of the gates B1, K1, L1; the flip-flop C 1 and 2, the binary ring H 1, 2; and the matrix of gates D1, L2, E1, E2) detects the initial signs of the numerator and denominator and, thus, determines whether the denominator is to be added or subtracted and whether +1 or -1 is to be put into the quotient. In the case of square rooting, after the process is started these circuits serve exactly the same purpose as in

division; that is, after an over-draft the arithmetical process must be changed from addition to subtraction (or vice versa) and the sign of the two's added into the denominator accumulator must be changed.

In period 1 of the process (division or square rooting) the gate D6 is opened by the program ring stepping to stage B.

If the denominator is negative, the negative static output of the PM-Clear unit of the denominator accumulator causes gate B1 to open. If the numerator is negative the static output of the negative stage of the PM ring of the numerator accumulator causes gate K1 to open. Thus, when the program ring steps to stage B a general pulse (GP) passes gate D6, turns the inverter I5 off and may pass gates B1 and K1 (depending upon the signs of the numerator and denominator).

Thus, after the program ring has reached stage B there are four possible situations as illustrated in the following table.

TABLE 6-2b

Numerator Sign	Denominator Sign	Matrix gate on	Result
+	+	E1	B10, G8, E13 are open. B10 passes a pulse which sets the D ₅ receiver causing the denominator to be subtracted.
+	-	D1	B11, H8, F13 are open and denominator will be added.
-	+	E2	B11, H8, E13 are open.
-	-	D2	B10, G8, E13 are open

Note that the arrangement of the gate tubes in this circuit is not the usual plan followed elsewhere in the ENIAC. Usually, there is an inverter between two gates. If the first gate tube begins to conduct it causes the inverter to go off. The resulting positive signal causes the second gate tube to conduct (assuming the other control grid is sufficiently positive). Here in the sign indication circuit (the same is true in the overdraft circuit, see section 6.2.4.) there is no inverter between the gate tubes. The plates of E1 and D2 are connected to one control grid of the gate tubes B11, H3, and F13. Thus, if gate E1 or D2 is conducting the grids of the three gates are held below cut-off and none of them can conduct. On the other hand, if neither E1 and D2 are conducting then their plate potential is relatively high and the gates B11, H3, and F13 will conduct if a relatively positive signal is applied to their other control grids.

Note that the denominator flip-flop is changed only at the beginning of the process, that is, it does not change its state during the process of division or square rooting. On the other hand, the numerator ring is stepped at the start for negative numerators and, in any case, is stepped during each shift sequence. At the end of the process the clear pulse (C1) arrives from the clearing circuits and resets the flip-flop and clears the numerator binary ring.

6.2.4. The over-draft circuit

The over-draft circuit is another matrix of gates similar to that in the sign indication circuit. This matrix is fed by the output of the numerator ring and by the static outputs of the PM ring in the numerator accumulator. The setting of the numerator ring is fixed during the process of addition or subtraction (in both division and square rooting) and its setting

depends upon the original sign of the numerator and the number of shifts which have occurred. When the PM sign of the numerator changes indicating an over-draft the static leads to the overdraft circuit change their potential causing a different gate to conduct.

As explained in the next section (6.2.5.) the add-subtract cycle takes two addition times. Thus, there is a full addition time after each trial addition or subtraction for the PM static lines from the numerator accumulator and the over-draft circuits to set up.

Thus, the sign indication circuits remember the sign of the denominator by the denominator flip-flop (remains unchanged throughout the whole process) and the sign of the numerator (by the numerator binary ring) (changes after each over-draft); and the over-draft circuit detects a change in sign of the numerator (or radicand in case of square rooting).

After the program ring has reached stage B (in period I), allowing the numerator ring to be stepped if necessary, gate G2 will be conducting if the numerator is positive, or else F1 in case the numerator is negative. Then gate D12 is closed and gate D11 is open. Gate D11 being open leads to the production of a pulse P which causes the add-subtract cycle to take place. When an overdraft occurs F2 or G1 is conducting, causing gate D11 to close and D12 to open. This leads to a shift sequence, that is the numerator is sent to the shift accumulator and then transmitted back through a shifter which moves it one place to the left.

6.2.5. The add-subtract circuit

The add-subtract circuit consists essentially of five receivers and their associated gates and inverters. These five receivers are (1) D_A which programs the denominator accumulator to transmit the denominator over its add

output, (2) D_S which programs the denominator accumulator to transmit the denominator over the subtract output, (3) N_A which programs the numerator accumulator to receive on α (this receiver is on the gate chassis instead of on a plug-in unit), (4) Q_γ which programs the quotient accumulator to receive on γ , and (5) D_γ which programs the denominator to receive on γ . Receiver Q_γ is used only in the process of division and receiver D_γ is used only in the process of square rooting.

At the start of an add-subtract cycle a P pulse passes gate B10 or gate B11, turns off the inverter B12 or B13, and activates the D_S or the D_A receiver, respectively. These receivers are reset by a signal from the buffer C5 or the gate D4. If the receiver D_S is activated the fast buffer output from a cathode follower goes (by way of interconnecting cables) to the common programming circuits of the denominator accumulator causing that accumulator to transmit over its subtract output. The slow output of the D_S receiver goes through the inverter C11 and opens the gates G11 and G12. The receiver D_A operates in a similar manner causing the denominator to be transmitted over the add output of the accumulator and the gates H11 and H12 to be opened.

The same P pulse which causes the D_A or D_S receiver to be activated also activates the N_A receiver (C, D 7, E7, F7, D8). The output of the cathode follower F7 goes to the common programming circuits of the numerator receiver and causes it to receive on α . The slow output goes through the buffer and inverter E7 and L8 to open the gates L9 and L10.

L9 or L10 pass square root pulses (SRP) or division pulses (DP) which set the D_γ or Q_γ receivers, respectively. The division pulse (DP) which passes L10 to set the Q_γ receiver also passes G11 or H11 to set the +1 or the -1 receivers in the numerical circuits (see section 6.3.) Similarly, in the process

of square rooting the SRP which activates the D_y receiver also passes G12 or H12 to set the +2 or the -2 receiver.

The slow buffer outputs of the D_y and the Q_y receivers join and connect to the grid of the inverter C10. Thus, when either D_y or Q_y is activated the inverter C10 will go off, the buffer E6 on, and the inverter F3 off giving a positive signal to the gates D11 and D12. If this addition or subtraction did not produce an overdraft gate D11 will be open, the inverter D10 will go off opening D9. This gate passes a general pulse (GP) producing another P pulse which starts another add-subtract cycle. If there has been an overdraft then gate D12 conducts starting a shift cycle (see section 6.2.8.)

6.2.6. The round-off circuit

The round-off procedure consists of subtracting the denominator from the numerator five times (in the case of square rooting, twice the square root is subtracted five times from what remains of the radicand in the numerator accumulator). If there is an over-draft nothing is done. If there is no overdraft then, depending upon the signs and whether the process was division or square rooting, a +1, -1, +2, or -2 is added to the quotient or to the denominator (twice the square root).

The round-off procedure occurs during period III (see PX-10-305 and PX-10-306) which is inaugurated by coincidence between the position of the quotient-place ring and the position of the root-divide-places switch as detected by one of the gates A41, B41, C41, A42, or A43. The subtraction (or addition) is started by a round-off pulse (ROP) being gated by C8 when the program ring is at stage B. This activates the N_a and the D_A or D_S receiver (the Q_y or D_y and the ± 1 or ± 2 receivers are not activated since no DP or SRP pulses are produced in period III). Since general pulses are not produced in this period, the D_A or D_S and the N receivers are not reset until the ring reaches stage 5.

At that time a reset signal is produced by an ROP pulse being gated by D4. When the program ring reaches stage 6 an ROP pulse is gated by J13, and if there has been no over-draft this pulse is passed by gate K12.

The divide-root flip-flop remembers whether the process was square rooting or division and accordingly decides whether to send ± 1 or ± 2 and whether to send them to the denominator accumulator or to the quotient accumulator.

In case of division the pulse which may be passed by gate K12 passes gate J10 to set the Q_y receiver and it passes gate J8 to activate the +1 or the -1 receiver (depending upon the signs this pulse may pass gate G8 to activate the +1 receiver or else it would pass the gate H8 to set the -1 receiver).

6.2.7. The root correction circuit

In the process of square rooting, after an over-draft has occurred it is necessary to correct the number appearing in the denominator accumulator. In the case of a subtraction cycle the number being subtracted (that is, the number in the denominator accumulator) is being increased by two each time. After an over-draft occurs one more two is added on, then one must be subtracted at the same place and another one must be subtracted in the next place to the right. If it is an addition cycle, then two is being subtracted from the number in the denominator each time, and after the over-draft one more two is subtracted, then one is added on and another one added in the next place to the right.

The circuits are so arranged that there is always one more "two" added or subtracted after the actual over-draft occurs. The root correction circuits take care of the adding or subtracting the "one".

After an overdraft occurs a general pulse (GP) passes gate E9 starting the shift process, setting the flip-flop (A, F 10) of the D'_y receiver, and passing gate H9 or G9 to set the +1 or the -1 receiver. These receivers remain activated for two addition times, since the root reset signal is not produced until the N'_y receiver is set, opening gate C11. The quotient place ring is automatically stepped (by gate L45 being opened) in between, so that the first ± 1 goes into one place in the answer and the next one goes into the next place to the right.

6.2.8. The shift circuit

When an over-draft occurs gate E9 is opened. This passes a general pulse (GP) which goes through the inverter F9 and sets the N_A and the S_a receivers. These receivers cause the numerator to transmit on add and clear, and the shift accumulator to receive on α . The slow buffer output of the S_a receiver goes through the inverter L8 to three gates. One of these gates, L1, passes a central program pulse which steps the numerator ring changing the sign in the sign indication circuits in preparation for the next add-subtract cycle. Another gate, L45, passes a 1' pulse (1'P), coming from gate F6, which goes to the pulse standardizer L-J, 11 and thence to step the quotient place ring. The third gate, K7, passes a central program pulse which activates the S_A and the N'_a receivers. These receivers cause the number now in the shift accumulator to be transmitted and cleared and received by the numerator accumulator.

The slow buffer output of the N'_a receiver goes through the inverter C10 to open the gates C9 and C11. C9 passes a general pulse (GP) to produce a P pulse which starts the next add or subtract cycle. C11 passes a general pulse to produce a root reset pulse which is essential to reset the D'_y and the +1 or -1 receivers in the case of square rooting. In the case of division this circuit is not used since division pulses are passed by the buffer C12 to pro-

duce a root reset pulse each addition time.

6.2.9. The interlock and clear circuits

These circuits consist of three flip-flops and associated gates and inverters. One flip-flop (H, J48) remembers whether the interlock signal has arrived or not (the interlock signal is the output program pulse for the last operation of the sequence of computations which goes on simultaneously with the root or division process). Another flip-flop (K, J 50) remembers the fact that the division or root process is finished. These two flip-flops open gates J49 and H50 which pass a central program pulse serially setting the flip-flop G, F 50. The interlock flip-flop H, J 48 may be by-passed in case the interlock switch is set at "NI". In this case the CPP passes gate K49 instead of gate J49. The pulse passed by H50 resets the flip-flop K, J 50.

The output of flip-flop G, F 50 opens gate 63 in the activated transceiver and gate F49. A CPP passes gate F49 and the inverter E49 to provide the Cl' pulse. Thus, Cl' is a positive pulse. In some places a negative pulse is needed for the clearing action so the Cl' pulse goes through a buffer E48 to produce the Cl pulse—a negative pulse.

The Cl' pulse does the following:

(1) May pass gate L48 (depending upon the position of the corresponding interlock switch) to reset the interlock flip-flop H, J 48.

(2) Turns on the buffer 48 causing the program ring to clear back to stage A.

(3) Turns on the buffer F3 resetting the flip-flop E 4, 5.

(4) Turns on the buffer C13 producing a root reset pulse which

resets the D_y receiver (E, F 10) and the +1 and -1 receivers.

The C1 pulse does the following:

- (1) Resets the flip-flop G, F 50.
- (2) Resets the denominator flip-flop C 1, 2.
- (3) Turns off the inverter K2 causing the numerator binary to be cleared.

6.2.10. The initial clear

The initial clear gate opens gates E50 and K48. E50 passes a CPP to the inverter E49 producing the C1' pulse (see above). The C1' pulse not only passes buffer E48 to produce the C1 pulse but also passes gate K48 to reset the interlock flip-flop H, J 48. The action of the C1 and C1' pulses in this case is exactly as described in the section above.

6.3. NUMERICAL CIRCUITS

The numerical circuits comprise the quotient place ring and its associated gates, the L1, -1, +2, and -2 receivers, the pulse gates. All of these circuits are located on the lower right hand corner of the block diagram PX-10-304.

6.3.1. The quotient-place ring

The quotient place ring causes the ± 1 or ± 2 which go to make up the quotient or the square root to arrive in the proper decade of the quotient or denominator accumulator. Also this ring causes the division or root process to be terminated when the proper number of places (as determined by the divide-root-place switch, see section 6.1.6.) in the answer have been computed. The ± 1 and ± 2 receivers open combinations of gates which pass groups (of the 1, 2, 2', 4, or 9 pulses) of pulses which represent the numbers +1, -1, +2, or -2.

The static output of each stage of this ring goes directly to one gate

tube and through an inverter to another gate tube. Thus, most of the gates connected to the ring are normally open and those connected via the inverters are normally closed. The ring closes to stage one (tube 29). Then, normally (after initially clearing) gate K42 will be open and all of the gates B42 to L42 will be open except K42. As the ring steps through various positions, one of the gates B42 to L42 is always open, and all except one of the gates B42 to L42 are conducting.

In the following discussion assume that the quotient place ring is at stage 1 and the cases where the receivers +1, -1, +2, and -2 are each activated will be discussed in succession.

(1) +1 receiver is activated. This causes gate L46 to be open passing a one pulse (1P) through the inverter and buffer system K45, J45, and H45. Of the gate tubes B to L42 only K42 is open. Thus the one pulse passes this gate to the inverter K44 and appears on the ninth channel of the output plug.

(2) -1 receiver is activated. This causes gates B45, G to K46 to be opened. Gate G46 passes the nine pulses (9P) through the buffer and inverter system F45, E45, D45, and C45 to the gate tubes B to L43. Since all these gate tubes except K43 are open nine pulses appear on all channels except channel nine (including the P4 channel). The gates H to K46 pass the 2P, 2'P, and the 4P through the buffer and inverter system K45, J45, and H45 to the gate tubes B to L42. Since only K42 is open this gives eight pulses on channel nine. The gate B45 passes the 1'P directly to the inverter B44 of channel one. Thus, before the 1'P arrives the quotient has received the number

M98999 99999.

After the 1st P arrives the accumulator has received the number

M99000 00000,

which represents the number -01000 00000.

(3) +2 receiver is activated. The gate L46 is open. This gate passes the 2P to the buffer and inverter system and then to the gates B to L 42. Gate E42 passes these pulses into channel nine.

(4) -2 receiver is activated. Gates E46 and G to K 47 are open. L7 passes nine pulses into the PM channel and through all the gates B to L 43 except E43. Gates H, J, and E47 pass the 1P, 2P, and the 4P to give seven pulses through gate E42 into the ninth channel. E46 passes the 1st P into the first channel. Before the 1st P arrives the denominator accumulator receives

M97999 99999.

After the 1st P arrives the denominator accumulator has received

M92000 00000,

which represents the number -02000 00000.

The quotient place ring is stepped by a 1st P passing gates F6 and L45. Gate F6 is open except in period III (the round-off period) and gate L45 is opened once each shift cycle.

The quotient place ring also performs a second function. Suppose the places switch is set at eight. Then, when the quotient place ring reaches stage seven (there may be eight digits in the quotient) the gate A41 (just under the pulse source circuits) will conduct turning the inverter I50 off and opening gate I4. After the add-subtract cycles corresponding to this position of the quotient place ring have taken place (producing possibly an eight digit quotient or square root), the next shift cycle starts. At this time the output of gate I4 passes gate I4 sending the pulse source flip-flop (I4, 5). This closes the

gate F6 and thus the quotient place ring is stepped no farther, even though the shift of the number in the numerator accumulator takes place. This means that the number which may be added or subtracted as a result of the round off procedure is put in this same place (that is, in channel three).

6.4. EXAMPLES

The following table gives the setting of the program control switches in the different examples:

	Example 1	Example 2
Numerator receiver switch	a	a
Numerator clear switch	C	C
Denominator receive switch	β	O
Denominator clear switch	C	O
Interlock switch	I	NI
Answer disposal switch	1	1
Round-off switch	RO	RO
Root-divide place switch	D 8	R 10

6.4.1. A division example

Addition and
pulse time

Discussion

0.17

Program pulse arrives at buffers 67, 68, and 69. The output of buffer 67 activates the D_8 receiver. The output of buffer 68 activates the N_2 receiver. The output of buffer 69 activates the transceiver in the divider. The output of the cathode follower 64 opens the gate K41. One of the buffers 61 gives a signal through the interlock switch to open the gate L48. The other buffer 61 gives a signal through the root-divide and round-off switch to open gates K5 and K6.

Addition and
pulse timeDiscussion

- 1.1 to 1.10 The numerator and denominator accumulators are receiving the numerator and denominator. (It is assumed that the program pulse which activates the divider is used to cause the transmission of the numerator and denominator from whatever units contain them.
- 1.17 A general pulse (gated CPP) passes gate K6 to provide the first division pulse (DP). This DP passes gate A10 to step the program ring to stage B. The output of stage B opens gate D6. During this time the PM static lines from the numerator and denominator to the sign indication circuits are setting up.
- 2.17 Another DP steps the ring to stage 1 causing gates B8, A7, and B7 to open. A general pulse (GP) passes gate D6 which may or may not step the numerator ring and/or the denominator flip-flop depending upon the signs of the respective quantities.
- 3.17 A GP passes gate A7 clearing the program ring back to stage A. A GP passes gate B7 setting the flip-flop A, B 6 closing the gates A10 and A11. A DP is passed by gate B8 producing a first P pulse. This P pulse activates the N_a receiver and either the D_A or the D_S receiver (depending upon the signs). Activating the N_a receiver causes gate L10 to open. Say that the signs are alike then the D_S receiver will be set and thus gate G11 opened.
- 4.17 A DP passes gate L10 and activates the receiver Q_y . This causes gates D11 and D12 to be opened. A DP passes gate G11 setting the +1 receiver. A GP passes the buffer C5 and resets the N_a and the D_S receivers.
- 5.1 Gate L46 passes a one pulse (1P) which passes gate K42 to go into the ninth decade of the quotient accumulator.
- 5.17 A DP passes the buffer C12 to reset the +1 receiver. The Q_y receiver is reset by a CPP. Assuming there has been no over-draft gate D9 passes a GP to produce the next P pulse. This P pulse sets the N_a and the D_S receivers.
- 6.17 Same as 4.17.
- 7.17 Assuming there has been an over-draft the gate E9 passes a GP which sets the N_a and the S_a receivers. This causes gates L45, K7, and L1 to be opened.
- 8.1 to 8.9 The numerator is being transmitted to the shift accumulator.

Addition and
pulse timeDiscussion

- 8.10 A 1'P passes gate F6, L45 and steps the quotient place ring to stage 2. The numerator accumulator clears.
- 8.17 A CPP passes gate K7 activating the S_a and N_a receivers. The activating of receiver N_a opens the gate C9.^a
- 9.17 A GP passes gate C9 to produce a P pulse. This starts an add cycle (since the numerator ring has been stepped). That is, this P pulse activates the N_a and the D receiver. Activating the D_a receiver causes gate H11 to be opened.
- 10.17 As in 4.17 the Q_v receiver is activated and a DP passes gate H11 to set the -1 receiver.
-
- 0.10 A 1'P passes gates F6 and L45 to step the quotient ring to stage 7. The N_a and S_a receivers are set. Gate A41 begins to conduct opening gate E6.
- 1.17 Gate C9 passes a GP to provide a P pulse which activates the N_a and the D_s receivers.
- 2.17 A DP passes gate L10 setting the Q_v receiver. A DP passes gate G11 setting the +1 receiver. Assuming there has been an over-draft gate D12 begins to conduct opening gate E9.
- 3.17 A DP resets the +1 receivers. A GP passes gate E9 activating the S_a and the N receivers. This pulse from E9 passes E6 to set the pulse source flip-flop E 4, 5. Thus, this is the last addition time in which general pulses (GP) and therefore division pulses (DP) are produced. As before the output of the S_a receiver opens gates K7, L45, and L1.
- 4.10 Gate F6 is now closed so no 1'P is passed.
- 4.17 CPP's pass gates K7 and L1 to set the S_a and the N receivers and to step the numerator ring, respectively. A CPP passes gate F5 to produce the first IIIP pulse. This IIIP pulse goes through the buffer A12 to step the program ring to stage B. It also passes gate K5 to produce a round-off pulse (ROP).
- 5.17 An ROP pulse (a IIIP gated by K5) passes gate C8 to produce a P pulse which activates the N_a and D receivers. A IIIP pulse passes the buffer A12 to step the program ring to stage 1.

Addition and
pulse timeDiscussion

- 6.1 The denominator is added to the numerator.
to
6.9
- 6.17 A IIIP pulse steps the program ring to stage 2. The N_a and D_a receivers are not reset since there are no GP's to pass the buffer C5.
- 7.17 A IIIP steps the program ring to stage 3.
- 8.17 A IIIP steps the program ring to stage 4.
- 9.17 A IIIP steps the program ring to stage 5. This opens the gate D4.
- 10.1 The denominator is added to the numerator for the fifth time.
to
10.10 Suppose that this does not produce an overdraft in which case gate K12 remains open.
- 10.17 An ROP pulse passes gate D4 to reset the N_a and the D_a receivers. A IIIP steps the program ring to stage 6, opening gates E3 and J13.
- 11.17 An ROP pulse passes gate J13, K12 (assuming there was no overdraft), and gates J8 and J10. The output of J10 sets the Q_y receiver. The output of J8 is passed by gate F8 or G8 depending upon the signs and sets the +1 or the -1 receiver. A IIIP steps the program ring to stage 7. A CPP passes E3 to reset the pulse source flip-flop.
- 12.1 +1 or -1 is added into one decade of the quotient accumulator.
to
12.10
- 12.17 A CPP passes F4 and K6 to produce a DP which resets the +1 or the -1 receiver.
A CPP passes L50 to set the flip-flop K, J 50.
-
- (Wait for interlock pulse)
- 0.17 Interlock pulse (program output pulse of some other unit) turns on one of the buffers F 46-48 and G48 setting the flip-flop H, J 48.

Addition and
pulse timeDiscussion

1.17
(13.17)*

A CPP passes J49 and H50 to set the flip-flop G, F 50 and reset K, J 50. Flip-flop G, F 50 causes gate 62 in the transceiver to open.

2.10
(14.10)

The carry-clear gate passes gates A48 and A49 and appears at terminals on the front panel.

2.17
(14.17)

A CPP passes F49 to produce the C1 and C1' pulses.

The C1' pulse does the following

- (1) passes gate L48 to reset H, J 48.
- (2) passes buffer A8 to clear the programming
- (3) passes buffer F3 to reset the pulse source flip-flop E 4, 5.
- (4) passes buffer C13 to reset the D_y receiver (E, F10, F11, E11, E12) and the ± 1 receivers.

The C1 pulse does the following

- (1) the flip-flop A, B 6 to reset.
- (2) resets the denominator flip-flop C 1, 2.
- (3) turns off the inverter K2 clearing the numerator binary ring.

A CPP passes gate 68 in the transceiver resetting it and being transmitted.

A CPP passes D46 to activate one of the answer disposal transceivers.

6.4.2. A square root example

Addition and
pulse timeDiscussion

0.17

Program pulse arrives at buffers 67, 68, and 69.

The output of buffer 68 activated the N_d receiver, and the output of 69 activates the transceiver in the divider.

The output of the cathode follower 64 opens the gate A43. One of the buffers 61 gives a signal through the interlock switch to open the gate K49. The other buffer 61 gives a signal through the root divide and round-off switch to open gates K3 and K4.

*Read this time if interlock signal arrives before completion of division process.

Addition and
pulse timeDiscussion

- 1.1
to
1.10
- The radicand accumulator (same as numerator) is receiving the number to be square rooted.
- 1.17
- A GP (A CPP passes by gate F4) passes gate K3 to produce the first square root pulse (SRP). This SRP passes gate A11 to step the program ring to stage B, opening gate D6.
- 2.17
- Another SRP steps the program ring to stage 1 causing gates A7, B7, K6, and G7 to open. A GP passes D6 but has no effect on the denominator flip-flop since the denominator contains the number +00000 00000 at this time. If the radicand were negative the binary ring would be stepped.
- 3.17
- An SRP pulse passes gates K8 and G7 setting the D_y and the +1 receivers, respectively.
A GP passes gate A7 clearing the program ring back to stage A.
A GP passes gate B7 setting the flip-flop A, B 6 causing the gates A10 and A11 to close.
- 4.17
- The output of the D_y receiver passes gate D11, opens gate D9 which allows a GP to be passed producing the first P pulse. This P pulse activates the N and the D_s receivers (since the denominator consists of +1 in a certain decade).
- 5.1
to
5.10
- The +1 in the denominator is subtracted from the radicand.
- 5.17
- A GP resets the N_a and the D_s receivers (from buffer C5).
An SRP passes gate L9 to set the D_y receiver and gate G12 to activate the +2 receiver.
- 6.1
to
6.10
- +2 is added into the denominator giving 3.
- 6.17
- A CPP resets the D_y and the +2 receivers.
Assuming there is no overdraft gate D11 is conducting and thus, D9 passes a GP to produce the next P pulse.
- 7.17
- An SRP activates the D_y and the +2 receivers.
Assuming there is an over-draft this time gate D12 conducts opening gate E9.
- 8.17
- A GP passes gate E9 and sets the S_a and N_a and D_y receivers, and it passes gate G9 to set the -1 receiver.

Addition and
pulse timeDiscussion

- 9.1 -1 is added to the +5 that was in the denominator accumulator.
to The radicand is transmitted to the shift accumulator.
9.10 A'P steps the quotient ring.
- 9.17 A CPP passes K7 to activate the S_A and the N_A receivers and
passes gate L1 to step the numerator ring.
- 10.1 -1 is again added to the +40 in the denominator accumulator
to giving +39.
10.10 The radicand is transmitted back (through a shifter) to the
numerator accumulator.
- 10.17 A GP passes gate C11 to reset the D_y and the -1 receivers.
A GP passes gate C9 to produce another P pulse.
-
- 0.10 A 1'P passes gates F6 and L45 to stop the quotient ring to
stage 9, causing gate A43 to conduct and, thus, opening gate E6.
- 0.17 The S_A and N_A receivers are set by a CPP through gate K7.
The numerator binary is stepped to minus (a minus radicand)
- 1.17 A GP passes gate C9 to produce a P pulse. This pulse activates
the N_A and the D_g receivers.
- 2.17 An SRP passes gates L9 and G12 to set the D_y and the +2 receivers,
respectively. Assuming there has been an overdraft gate E9 opens.
- 3.17 A GP passes gate E9 activating the S_A and the N_A receivers, and
passes gate E6 to set the pulse source flip-flop E4, 5. Thus,
this is the last addition time in which GP pulse, and therefore,
SRP pulse will be produced.
- 4 What happens during these addition times is exactly a repetition
to of what happens in the case of division (explained in example 1).
11
- 12.17 A CPP passes gates K49 and H50 (opened by the program ring being
at stage 7) and sets the flip-flop G, F 50.

addition and
pulse timeDiscussion

13.17

A CPP passes gate F49 producing C1 and C1' pulses. The C1 pulse resets the coincidence flip-flop G, F 50, and clears the quotient ring and the numerator ring. The C1' pulse clears the program ring, resets the pulse source flip-flop (E 4, 5), and resets the D_y and the +1 and -1 receivers.

The C1 pulse resets the flip-flops A, B 6, and C 1, 2. The output of the coincidence flip-flop causes the gate 62 in the activated transceiver to conduct, which in turn opens the gates B48, one of the gates C46, D46, D47, or E47 (for answer disposal), and gate 68 in the transceiver.

14.10

The carry-clear gate passes gate B48 and clears the numerator accumulator.

14.17

A CPP passes gate 68 and is transmitted as an output program pulse.

A CPP passes gate D46 and activates the first answer disposal receiver.

VII FUNCTION TABLE

There are three function tables in the ENIAC; each stores the values of a function for 104 values of the argument. Associated with each function table is a portable function table supporting an array of switches on which the operator can set the values of the function. For each value of the argument the portable table has twelve digit switches and two PM switches (thus, the portable table has 1248 digit switches and 208 PM switches).

Panel #2 (the right hand panel) contains eight master digit switches and two master PM switches. These are for setting any digits (as many as eight) that are the same for all values of the argument. The PM master switches can be used when all function values set up in the table are of the same sign, making it unnecessary to set the PM switches of the table.

Thus, altogether, for each value of the argument there are twenty digits (eight of which are the same for all arguments and twelve of which can vary from argument to argument) and two PM signs (determined either by the master PM switches or by the settings of the various PM switches on the portable table). The two PM signs enable the operator to set up the values of two functions for each argument allotting the twelve variable digits and the eight master digits to the two functions in any manner. This allotting of digits to the two functions requires special adapters at the two function table outputs (see Section 11.6.5.).

Four of the master switches (A_1 to A_4) feed lines 7 to 10 of the A output. Master switches B_1 to B_4 feed channels 7 to 10 of the B output. The PM_1 master switch feeds the PM channel of the A output and PM_2 master switch feeds the PM channel of output B. The left hand six columns of switches on the portable table feed channels 1 to 6 of the A output. The right hand six columns

of switches feed the lines one to six on the B output.

If one desires to transmit any other combination of these channels into one digit trunk then the appropriate adapter must be constructed (see Section 7.3 9.).

The function table transmits in five addition times the functional value (or any of four neighboring functional values depending upon the setting of the argument switch--this is for interpolation purposes). By using the repeat switch the function table may transmit the functional value n times ($1 \leq n \leq 9$) in $n+4$ addition times.

7.0. INTRODUCTION

In the upper right hand corner of the block diagram PX-7-304 appear the switches of the portable function table. In the upper left hand corner are the units and tens argument rings. Between these and the table switches are the table input gates or table selectors. Below the argument rings (left center of the diagram) is the program ring, and below this, two program control circuits (there are nine other program control circuits) are illustrated. At the bottom center of the diagram are the pulse gates which pass combinations of the 1, 2, 2', 4, and 9 pulses to make up pulse representations of the digits 0, 1, 2, ..., 9. To the right of this are the master switches (which are used to set up digits which do not change for all 104 values of the argument) and in the right hand corner are the transmitter circuits.

The table output gates and all circuits below them (on the diagram) including the pulse gates are located on the right hand panel (panel #2) of the function table. The switches (in the upper right corner) are on the portable unit. All other circuits (including the rings, the flip-flops, and the program

control circuits) are located on the left hand panel (panel #1) of the function table.

There are three complete function tables. Each one is identical with the others so anything said in the following discussion applies to all three.

For purposes of discussion the circuits of the function table are divided into three types. The program control circuits comprise the eleven transceivers and their associated switches. The common programming circuits comprise the program ring and its associated gates, the argument flip-flop, the subtract flip-flop, and the add flip-flop. The balance of the circuits make up the numerical circuits. The numerical circuits include the argument rings, the table input gates, the portable table, the table output gates, the pulse gates, the constant switches, PM master switches, delete switches, subtract pulse switches, and the output transmitters.

7.1. THE PROGRAM CONTROL CIRCUITS

7.1.1. The Transceivers

There are eleven transceivers located in the #1 panel of the function table. These are standard, that is, they are exactly the same as those used in the accumulators and most other units of the ENIAC.

7.1.2. The Argument Reception Switch.

The buffer which feeds this switch (that is, the cathode follower in the transceiver) serves two functions, namely, to control the transmission of the argument and the stepping of the program ring. The argument reception switch has three possible settings controlling the reception of the argument from some other unit of the ENIAC. On all three settings the fast buffer out-

put (tube 64) of a transceiver goes to gates D49, E49, or F49, one of which passes central program pulses which step the program ring. If the switch of the activated program control circuit is set on NC, a central program pulse passed by gate J48 (opened by stage -3 of the program ring so that J48 is open at the beginning of the program) will turn inverter H48 off, and pass gate H46. The pulse will then go through the transmitter J-L 46, and appear on the front panel (terminal labeled NC, see PX-7-302). From there it can be taken (via jumpers and program trays) to some other unit of the ENIAC to program the argument transmission. If the switch were set at C the action would be similar except the output pulse would pass gate H47 and be transmitted from the transmitter J-L 47. Supposedly, the NC circuit would be used when the argument is not to be cleared in the transmitting accumulator, and C is to be used when it is to be cleared.

These circuits are controlled by the fast buffer outputs (tubes 64 and 65) of the transceivers. Since these outputs have a small time constant the input circuits to the gate tubes have extra capacity purposely added. This delays the opening of these gates; keeping them from opening in time to pass part of the same CPP which activated the transceiver.

7.1.3. The Program Switch.

Deck 1 of the program switch determines whether plus or minus the functional value is to be transmitted. When set on A (add), and a program control is activated, the output of tube 61 in the transceiver causes the inverter E48 to stop conducting, opening the gate E47. When the ring is in stage zero this gate passes a pulse which sets the add flip-flop (tubes C46, 47). If the program switch is on S, then inverter E48 (the other triode) stops conducting, opening gate E46. Then, when the ring is on stage zero the subtract flip-flop

D46, 47 is set. The timing of these operations is illustrated in section 7.2.1.

Deck 2 of the program switch determines whether the functional value itself or one of the four neighboring values is to be transmitted. If the reader will check the connections from the argument rings to the switches of the table he will note that the table number is exactly two less than the number registered in the argument rings. Thus, if x denotes the argument then normally the function table would transmit $f(x-2)$. The number transmitted and the corresponding setting of the program switch is as follows:

Program switch setting	Number transmitted	Number in argument rings
-2	$f(x-2)$	x
-1	$f(x-1)$	$x+1$
0	$f(x)$	$x+2$
+1	$f(x+1)$	$x+3$
+2	$f(x+2)$	$x+4$

If the program switch is set at +1, for example, gates H44 and J44 will be opened by the output of the buffer 61 of the transceiver. When the program ring is at stage -1 gate E42 will be opened and three pulses will pass H44 and J44 through the inverter E44 and gate E42 and into the units argument ring. This changes the argument from x to $x+3$ and the function table will now transmit $f(x+1)$. Note that stage -1 of the program ring must open gate E42 in time to pass a 1P. Since the gate is physically close to the ring there is no difficulty in doing this with the usual two to one safety factor.

7.1.4. The Repeat Switch

This switch determines how many times the functional value is transmitted. If it is set at 3 (as illustrated) the functional value will be transmitted once when the ring is set at stage one, again at stage two, and the third time at stage three. The output of stage three (which is now positive) will go through terminal three on the repeat switch and open gate 62 in the transceiver. This causes the inverter 65 to go off and opens gate 68 giving an output program pulse at the end of this addition time. The output of the buffer 65 turns off the inverter D48 opening gates A48, B48, and C48. These pass central program pulses (CPP) which clear all three rings and reset all three flip-flops.

Thus, the functional table will transmit a functional value n times in $n+4$ addition times where n is any number between one and nine. Note that the accumulator which is to receive the function must be programmed to receive during either the whole $n+4$ addition times, or during the last n of the $n+4$. Consequently, if it is programmed simultaneously with the function table, it can receive the function only 5 times using a single transceiver. If, however, it can be programmed 4 addition times later than the function table, the setting of its repeat switch can be the same as that of the function table, and the function table can transmit to it the full 9 times.

7.2. THE COMMON PROGRAMMING CIRCUITS

7.2.1. The Program Ring

The program ring is a thirteen stage ring located on the left center of the block diagram. The following table illustrates what happens at each stage of the ring.

TABLE 7-2

Addition Time	Ring Stage	Effect
0	-3	Program pulse is received at a transceiver.
1	-3	At pulse time seventeen of this addition time the ring steps to stage -2, and, (depending upon the setting of the program switch), a pulse may be transmitted by J-L 46 or J-L 47. Usually the pulse transmitted here will be used to program the argument transmission from some other unit of the ENIAC.
2	-2	The buffer K48 will go on turning the inverter L48 off, opening the gates D42 and H42; allowing the argument to be received.
3	-1	Depending upon the setting of the program switch certain of the gates F44 to L44 may have been opened. Thus, from zero to four pulses are passing the inverter E44 and at this addition time these pass the gate E42 and enter the units argument ring. Gate F47 is also opened, allowing a 1 st pulse to set flip-flop B46-B47; this flip-flop, through buffer A46, turns off inverters B1 to L1 and A11, in turn permits one of the table input gates to conduct and energize one entry of table.
4	0	The output of the zero stage opens the gate G48. At pulse time seventeen of this addition time a central program pulse (CPP) passes this gate, turning off the inverter F48. Depending upon the setting of the program

switch, either gate E46, or E47 is open. Thus, the output of the inverter F48 sets either the add or the subtract flip-flop causing either the function value or minus the functional value to be transmitted during addition time 5 (and subsequent addition times for repeat switch settings above 1).

- | | | |
|---|---|---|
| 5 | 1 | Certain of the pulse gates are opened during this addition time, and the functional value is transmitted over the digit output (SX and SY in lower right hand corner). The output of stage 1 of the program ring connects to terminal 1 on all the repeat switches. |
| 6 | 2 | The functional value is transmitted a second time. |
| 7 | 3 | The functional value is transmitted for the third time, and (if the repeat switch is set on three as illustrated) gate 62 is opened in the transceiver. Then buffer 63 turns off inverter D48 opening gates A48, B48, and C48, causing the rings to clear and the flip-flops to be reset. |

7.2.2. The Argument Flip-Flop

The argument flip-flop B 46-47 is set by a 1' pulse passing gate F47. This gate is opened when the program ring is at stage -1. When the flip-flop is set it turns on buffer A47 which turns off the inverters B1 to I1 and A 11. This determines the time at which one of the table input gates conducts.

7.2.3. The Add and Subtract Flip-flops and the Pulse Gates

The following table gives a list of the gates opened and the effect when the add or the subtract flip-flop is set.

TABLE 7-3

Channel	Add						Subtract					
	1P	2P	2'P	4P	9P	Total pulses	1P	2P	2'P	4P	9P	Total pulses
0	-	-	-	-	-	0	-	-	-	-	L'4	9
1	K'4	-	-	-	-	1	-	K'1	K'2	K'3	-	8
2	-	-	J'2	-	-	2	J'4	J'1	-	J'3	-	7
3	H'4	-	H'2	-	-	3	-	H'1	-	H'3	-	6
4	-	-	-	G'2	-	4	G'4	-	-	G'3	-	5
5	F'4	-	-	F'3	-	5	-	-	-	F'2	-	4
6	-	E'1	-	E'3	-	6	E'4	-	E'2	-	-	3
7	D'4	D'1	-	D'3	-	7	-	-	D'2	-	-	2
8	-	C'1	C'2	C'3	-	8	C'4	-	-	-	-	1
9	-	-	-	-	B'4	9	-	-	-	-	-	0

The outputs of the pulse gates go to transmitting circuits, (amplifiers) (tubes B' to L', 5 to 10). The outputs of these transmitting circuits go to the various table output gates, the zero-nine channels go to the P and M terminals on the PM master switches, and through buffers B'63 to L'63 they all go to various terminals on the constant switches.

7.2.4. Use of the Function Table for Programming

The function table can be used to obtain program pulses on any of as many as 14 channels when a particular program control circuit is excited. The choice of output channel is controlled by any two digits of the number used as an argument, and registered in the argument accumulator.

To accomplish this, an adapter must be used in back of the function table on the cycling unit trunk. This adapter (PX-4-119) adds a central program pulse to the 9P lines of the function table panel #2.

Now, suppose that all the switches, on the portable table, for a particular argument are set to one; with the exception of one switch, which is set to "nine". Whenever the function table is programmed and the appropriate argument is stored in the argument accumulator a CPP will be transmitted over the channel corresponding to the switch which was set to "nine."

The nine pulse lines are used for this purpose since they also feed the PM switches. Consequently, the portable table can be used to give output pulses on any of fourteen channels (that is, twelve digit channels and two PM channels).

7.2.5. Initial Clear

The initial clear gate opens gates A48 to C48. The output of C48 resets the argument flip-flop (B46-47) and the add and subtract flip-flop (C46-47 and D46-47). Gates A48 and B48 operate in parallel to turn off three inverters A49 to C49. A49 and B49 in parallel cause the argument rings to clear. C49 causes the program ring to clear.

If the buffer 63 in any transceiver conducts, (as it will at the end of an operation for which its program control was activated), the inverter D48 stops conducting, opening the gates A48 to C48 giving the same effect as the initial clear gate.

7.3. THE NUMERICAL CIRCUITS

7.3.1. The Argument Rings

When the gates D42 and H42 are opened (at stage -2 of the program

ring) the two digits of the argument arrive over channels five and six of the input terminal and going through the pulse standardizers (J-L 42 and A41, B-C 42) step the units and tens rings to the proper position. When the program ring reaches stage -1, zero to four pulses may be passed by one of the gates F44 to M44 through gate E42, to step the units ring the corresponding number of positions. If this causes the units ring to step through stage nine gate M42 will be opened to pass the carry over pulse. This pulse goes through the inverter and buffer G42 and steps the tens ring one place. Note that the tens ring has eleven stages; also there is never any delayed carry-over problem. The argument will never exceed nine in the tens place but the carry over may give ten, thus, the extra stage.

Consider the control of the table selectors by the rings. After clearing (as illustrated) the rings each set at stage zero. This causes the inverters K2 and K26 to be non-conducting. Suppose that a program control is activated, and the argument is zero. Then when the argument flip-flop is set the inverter L1 conducts raising the potential of both grids of the table input gate (or table selector) K12. Incidentally, one control grid of several other table input gates will swing positively at this time, (for example, gates K13, K25, and K11, and others not illustrated), but since the other grid remains below cut-off, (because other inverters associated with the tens ring remain on), the tubes do not conduct. A similar statement is true for the gates A to K 12.

Thus, when the program ring is at stage -1, one of the table input gates begins to conduct and one of the horizontal buses of the portable table has a negative swing of potential.

The action of these inverters and gates is explained in some detail in section 1.2.3.)

7.3.2. The Table Input Gates

There are 104 table input gates corresponding to the argument values of -2, -1, 0, 1, 2, ..., 100, and 101. This gives a range of argument values of 0, 1, ..., 99 with the extra values on each end for purposes of interpolation. Of the two control grids of each gate tube, one connects to the output of an inverter controlled by the proper stage of the units ring, and the other control grid connects to the outputs of two inverters; one controlled by the tens ring, and the other by the argument flip-flop. In order for any particular gate tube to conduct all three inverters must be non-conducting. Thus, even though the argument arrives in the rings earlier, none of the table input gates conduct until the argument flip-flop is set at stage -1 of the program ring. Note that this flip-flop is set by a one primed pulse (1'P). The timing here is illustrated by table 7-4.

TABLE 7-4

Addition Time	Pulse Time	Activity
0	17	Programming pulse arrives at the function table.
1	17	Argument transmission is programmed and receiving gates (F47, G42) are opened.
2	17	Program ring steps to stage -1 opening gates E42 and F47.
3	1 to 5	Argument adjustment takes place by 0, 1, 2, 3, or 4 pulses passing gate E42.
	10	Argument flip-flop is set by 1'P.
	17	Program ring steps to stage 0 opening gate G48.
4	17	Program ring steps to stage 1 opening gate 62 in the transceiver (provided the repeat switch is at one) and a central program pulse passes gate G48 to set the add or the subtract flip-flop.
5	1 to 10	Functional value is transmitted.
	17	Central program pulse passes gate 68 in the transceiver to be transmitted and to reset flip-flop. CPP also passes gates A48, B48, and C48 to clear rings and reset flip-flops.

7.3.3. The Portable Table

The portable table is a switching/network built as a separate unit, and connects to the function table unit through two IBM type plugs. Since the portable table is on wheels, the operator may quickly interchange it with one connected to any other function table.

Each portable table mounts 208 PM (sign) indication switches (two for each argument value) and 1248 digit switches (12 for each argument value). There are 104 PM switches and 624 digit switches on each side of the portable table.

7.3.4. Table Output Gates

The nine terminal on each of the 104 switches in the sixth column of the portable table connects to the inverter B'11. The output of this inverter goes to the gate B'12, which when opened will pass either nine or zero (no) pulses depending on whether the associated program control is on add, or subtract program respectively.

The ten positions of the switches in each column go to ten inverters. Each output from the ten inverters goes to one grid of ten gates, the other grids being fed by the pulse gates.

Thus, if horizontal bus 11 is energized and the sixth column digit switch is at 7 (as illustrated) the inverter D'11 will cease conducting and the gate D'12 will open. This gate will then pass 7 or 2 pulses depending upon the setting of the argument switch of the associated program control circuit.

There are 120 inverters and 120 output gates on the digit channels. The two PM channels feed four more inverters and gates (C' to K' 61).

The outputs of the digit gates (labeled A5 to A10, and B5 to B10) go through inverters and buffers to transmitters, (these transmitters use a

616 in place of the usual 6V6) and then to terminals SX and SY. The outputs of the PM gates go to the PM master switches (PM₁ and PM₂ associated with the A and the B outputs respectively).

7.3.5. The PM Master Switches

The PM master switches make it possible to determine the sign for all the table entries at once instead of setting the individual PM switches on the portable function tables. This is useful only if all entries are of the same sign.

There is a PM master switch associated with each output (SX and SY). These switches determine the sign indication transmitted on the channel of the respective outputs. Each switch has three settings, Table, P, and M. The following table gives results of various settings of these switches.

Master switch setting	Pulses transmitted over the PM channel	
	Add flip-flop set	Subtract flip-flop set
P	0	9
M	9	0
Table	0 or 9 depending upon the setting of the corresponding PM switch on the portable table.	

7.3.6 The constant switches and the delete switches

There are eight constant switches, four associated with each of the outputs SX and SY. If the first few digits of a function are the same for all arguments used, these switches simplify the procedure for setting up the values of the function. Therefore, when some program control is activated the numbers set on these constant switches (or complements) will be transmitted over the corresponding channels regardless of the value of the argument.

The outputs of the transmitters associated with the pulse gates comes through buffers B'63 to L'63 to ten of the positions on each of these

switches. Two other terminals on each of these switches make available the outputs of the two PM master switches here. This is to help provide the proper complements.

The delete switches are provided on each of these channels in case the operator desires to transmit nothing on one or more channels.

7.3.7. The Subtract Pulse Switches

Since the complementation provided by the add or subtract flip-flops and pulse gates gives complements with respect to $10^n - 1$, it is necessary to provide a correction pulse to get complements with respect to 10^n . The correct pulse switches enable the operator to provide this correction pulse in any of six channels on each output, namely, A5 to A10 and B5 to B10.

The output of the subtract flip-flop goes through the inverter D45 to the gates A'64. The 1'P is passed by these gates through the inverter A'63 to the buffers A'61, A'62 to L'62.

These subtract pulse switches enable the operator to divide the 12 variable digits set up on the portable table into arbitrary groups and cause each group to give complements with respect to 10^n .

7.3.8. The output transmitters

The outputs of the constant switches go through the delete switches directly to transmitters. The outputs of the table output gates go through an inverter and a buffer to transmitters. Special adapters can be easily built to rearrange the outputs and allow transmission onto a single digit trunk.

If the operator desires, for example, to set up a ten digit function on the table and his function is such that the constant switches cannot be used then six of the digits can be obtained from channels A5 to A10. The other four must come from four of the channels B5 to B10 and a special adapter must

be used to get these ten digits onto one digit trunk.

7.3.9. Adapters

In designing an adapter for use on the function table outputs there are two points to watch. First, the function table outputs (which are to be used) are connected in a one-to-one manner to terminals corresponding to the trunk lines to be used. Secondly, if negative numbers are to be transmitted, then any unused lines, corresponding to accumulator decades between the PM unit and the first decade used, must carry 9 pulses in order to give the proper complements. This second objective can be accomplished by connecting the outputs of some of the master digit switches (A, to A_4 or B, to B_4) to the corresponding lines. The PM_1 and PM_2 positions of the master switches provides 9 pulses at the proper times.

If for any reason the master digit switches cannot be used for this purpose the adapter can be made to transmit the number onto the trunk using only channels adjacent to the PM line (line 11). In this case a shifter can be used on the input to the accumulator. The shifter provides for the extra "nines" needed for complementing purposes (see section 11.3.)

VIII. THE CONSTANT TRANSMITTER AND IBM READER

The constant transmitter stores eighty digits on relays and twenty digits on constant set switches. Provision is made for twenty PM signs, sixteen associated with the numbers stored on relays and four associated with the numbers set on the switches. One of these PM signs is associated with each five digits. Thus, the constant transmitter can store twenty five-digit numbers and their proper signs. Provision is made to associate certain groups in pairs to form ten digit numbers. In one addition time the constant transmitter can transmit to some other unit of the ENIAC any group of five or certain groups of ten digits and the associated sign.

Whenever it is desired to set up new constants on the relays in the constant transmitter, the IBM reader must be programmed to read a new card. This does not change the digits set on the constant set switches; these have to be changed manually.

The reader completely reads a card and stores the information on relays in the constant transmitter in 0.48 seconds. After about 0.3 seconds the starting circuits of the IBM reader are reset and will be able to remember a second signal to read (generally this fact is insignificant since computations cannot be started until the initial data is read into the constant transmitter and, also, there is no program output from the reader to start any computation until the end of the reading cycle). If in some manner it is arranged to program the next reading of a card before the first cycle is completed (this must not occur before say 0.4 seconds after the initial read program and this only allows a $3\frac{1}{2}$ safety factor) then, due to the clutch not dropping out, the reader will read a card in 0.36 seconds.

Thus, the reader can read normally as many as 125 cards per minute not allowing for any computations in between. On the other hand, since each IBM time unit corresponds to about 170 addition times, and there is an interval of about 1.2 units between the finish pulse and the dropping of the holding cam contact, it seems that even though the output of the reader is used to re-program the reader that this same pulse can be used to cause transmissions from the constant transmitter safely (safety factor = 2:1). During the period of 100 addition times after this pulse, numbers could be transmitted from the constant transmitter. By the device mentioned above the speed of reading can be increased to as much as 160 cards per minute.

The description given here will be in terms of the following diagrams:

- 1) Constant Transmitter Cross Section PX-11-116, 2) Constant Transmitter Block Diagram PX-11-307, 3) Constant Transmitter and Reader Cross section, and 4) IBM Reader Diagram PX-11-119. The discussion will be divided up into the following sections: 1) Constant transmitter program controls, 2) IBM reader program controls, 3) Numerical circuits of the constant transmitter, 4) IBM reader, and 5) Examples.

8.1. CONSTANT TRANSMITTER PROGRAM CONTROLS

8.1.1. The groups of numbers

As indicated above the constant transmitter stores twenty five-digit numbers and as many as twenty PM signs. These are divided into five-digit groups called A_L , A_R , B_L , B_R , ..., H_L , H_R , J_L , J_R , K_L , and K_R . The first sixteen groups A_L to H_R are read from IBM cards while the last four groups J_L to K_R are set on the constant set switches.

8.1.2. Transceivers

There are thirty transceivers in the constant transmitter. These are associated in groups of six. The first six transceivers control the first four five digit groups of numbers A_L to B_R . The next six control the groups C_L to D_R , et cetera. Finally, the last six transceivers control the groups J_L to K_R which can be set on the constant set switches (see panel two of constant transmitter, PX-11-303).

Two transceivers of a group of six are illustrated on PX-11-307.

These are for programs numbered one to six and control the first four five-digit groups of numbers. The output from the cathode follower (tube 64, see PX-5-30) of each transceiver connects to two decks of the associated constant selector switch. The cathode follower is used to drive the switch because fast operation of the circuit is required to make possible transmission of a constant during the addition time following the addition time in which the program pulse is received. The other outputs of the transceiver are unused.

8.1.3. The Program Control Circuits

Associated with the relays of groups one to four (likewise for five to eight, nine to twelve, and thirteen to sixteen) there are eighty-eight gate tubes. In each group there are four gate tubes for each of the five digits (as the 1, 2, 2', and 4 coded system is used to form the digits) and two gates associated with the PM indication. There are six constant selector switches associated with each such set of 88 gate tubes (switches one to six with groups one to four, for example). The output terminals of these switches go directly to the grids of the gate tubes.

Switches 25 to 30 are associated with the gates controlled by the constant set switches on panel two of the constant transmitter. There are only

64 gates associated with these switches since the gates associated with the correction pulse are omitted. (This means that the operator sets up complements here as complements with respect to 10^n and not 10^n-1).

Whenever a program pulse is received on the input terminal of a program control, at 11 say, the output of the cathode follower (tube 64 in the transceiver plug-in unit) goes to the two decks of the constant selector switch. The results of the various settings on this switch are given in the following table.

TABLE 8-1

Constant Selector Switch	Result	
	Deck 1	Deck 2
A _L	The cathode follower potential opens the PM gates A'1 and A'21.	The cathode follower potential opens the digit gates for group 1, that is gates B' to L' 1 and 21.
A _R	Gate A'41 (PM) is opened.	The PM gate A'62 and digit gates B' to L' 41 and 61 are opened. (A'61 controls the correction pulse).
A _{LR}	The PM gate A'1 is opened.	The PM gate A'62 and the digit gates B' to L' 1, 21, 41, and 61 are opened.
B _L	The PM gates A'2 and A'22 are opened.	The digit gates B' to L' 2 and 22 are opened.
B _R	The PM gate A'42 is opened.	The PM gate A'63 and the digit gates B' to L' 42 and 62 are opened.
B _{LR}	The PM gate A' 2 is opened.	The PM gate A' 63 and the digit gates B' to L' 2, 22, 42, and 62 are all opened.

Since the constant selector switches are connected in parallel, within any group of the same alphabetical letter "back circuits" would be created

should one switch be turned to L or R when another is turned to LR. For example, in the first group of six constant selector switches, if one is set at A_{LR} , whether can be set at A_L or A_R without transmitting superfluous digits (in the case of a positive number), or the extraneous transmission of 9P and 1'P over certain channels (negative number). This means that if the number stored on groups one and two relays is transmitted as a ten digit number, then at no other place in the computation can it be considered two five-digit numbers, or vice versa.

If an activated program control has its switch set to A_L , the five digits of group one will be transmitted on channels 6 to 10. If the number is negative nine pulses will be transmitted over the PM channel ($A'1$ turns off the inverter $A'11$ opening the gate L43) and the correction pulse will be transmitted over channel 6 ($A'21$ turns off the inverter $A'11$ opening the gate L45). In this case nothing is transmitted over channels one to five.

If an activated program control has its switch set at A_R the five digits of group 2 will be transmitted over channels one to five. If this number is negative nine pulses will be transmitted over channels six to ten and over the PM channel ($A'41$ turns off the inverter $A'51$ opening the gates F to K 45 and L44) and the correction pulse will be transmitted over channel one ($A'62$ turns off the inverter $A'61$ opening the gate A45). The nine pulses transmitted over channels six to ten give the complement with respect to 10^{10} and make it unnecessary to use a shifter in the digit transmission line.

If an activated program control has its constant selector switch set at A_{LR} the ten digits of groups one and two will be transmitted over channels one to ten. If the number is negative nine pulses will be transmitted over the PM channel ($A'1$ turns off the inverter $A'51$ opening the gate

143) and the correction pulse will be transmitted over channel one (A'62 turns off the inverter A'61 opening the gate A45).

The groups one to sixteen (or A_L to H_R) behave in a manner similar to above. The gates associated with the constant set switches (J_L to K_R) behave similarly except for the correction pulse (as explained above, or see Section 8.3.2.).

8.2. Reader Program Controls

The reader program controls are located in the initiating unit (see PX-9-307). The IBM reader can be caused to read a card, (provided certain conditions are fulfilled in the reader), either by a program signal arriving at terminal Ri on the front panel (PX-9-302) or by pushing the reader start button on that panel.

8.2.1. Starting

If the reader start button is pushed the resulting pulse goes through the special pulse standardizer (61 and 62, reader start unit, see PX-11-307). The output of the special pulse standardizer turns off the inverters 63 causing the buffer 72 (PX-9-104) to go on. This sets the flip-flops (65, 66) and (67, 68). The driving tube 64 goes on closing the starting relay (located in the constant transmitter (Panel #3)). If a program pulse is used to start the reader it comes in over Ri turning on the buffer 67 and setting the flip-flop (65, 66), but not the flip-flop (67, 68).

8.2.2. Resetting

After the reader starts to read the card a signal (a gate voltage) comes back over connection 129 (see PX-11-307) from the reader causing the flip-flop 65 and 66 to reset. This signal occurs early in the card reading cycle (when the minus indication is being read—before the digits are read

(see the cam time-table on PX-11-120). After this reset signal has arrived any subsequent program pulse arriving over R_1 sets the flip-flop and closes the starting relay. This causes the reader to continue and read the second card before stopping. The reset signal arrives from 800 to 1200 addition times after the print program signal.

8.2.3. The Finish Signal

Just as the IBM reader finishes reading the card a signal is sent over connection 127 to the special pulse standardizer (65, 66) causing the flip-flop 70 and 71 to be set. This opens the gate 69 and if the flip-flop 67 and 68 is then set the inverter 61 (Px-9-106) will go off opening the gate 62. The CPP passed here sets the flip-flop 63 and 64 opening gate 68. This passes a CPP which goes through the transmitter (65-67) to the reader program output R_0 . This same pulse goes through the inverter and buffer 69 and resets all three flip-flops.

The flip-flop 63 and 64 is a synchronized flip-flop, that is, it is set by a CPP gated by 62. The flip-flop 70 and 71 is not synchronized since it is set by a signal from the IBM reader. Thus, the gate 62 may be opened in such a way that it will pass only part of a CPP. If it fails to set the flip-flop 63 and 64 no harm is done since the next CPP will also be passed by 62 and will set the flip-flop 63 and 64. This flip-flop being set by a CPP will open the gate 68 in ample time for the next CPP. This arrangement insures that a standard synchronized program pulse is transmitted out or R_0 .

8.2.4. Interlock

Since the process of reading a card takes a very large number of addition times it is desirable to be carrying on part of the computation while this is being done. There will be a place in the sequence of computations

where the numbers in the constant transmitter are used for the last time. At this addition time the reader may be programmed to read the next card. Since, generally, it will not be known which process, that of reading the next card or that of completing the rest of the sequence of computation, will be finished first, an interlock feature is provided. The final output program pulse of the sequence of computation is plugged to R_1 . Thus, flip-flop 67 and 68 is set at the end of the sequence of computations while flip-flop 70 and 71 is set when the reader is finished. Only when both of these things have happened will the gate 69 conduct and open the gate 62, finally giving a program pulse out of R_0 .

The reader start button through buffer 64 also sets the interlock flip-flop (67 and 68). Therefore, when the reader start button is pushed the reader reads a card and a reader program output pulse is obtained at R_0 at the proper time.

The initial clear gate causes all of these flip-flops to be reset. Note that when the ENIAC is turned on the starting flip-flop (65 and 66) may come on in the set position and before a CPP arrives to reset it the reader may read one card.

8.3. NUMERICAL CIRCUITS OF THE CONSTANT TRANSMITTER

The numerical circuits of the constant transmitter comprise the sixteen groups of storage relays and their associated gates (A' to L' 1 to 10, et cetera), the constant and PM set switches (on panel 2) and their associated gates, the inverters (A' to L' 11, et cetera) and the pulse gates (A to K 41 to 44; A , E to K 44; L 43 and 44), and the inverters, buffers and transmitters (A to L 46 to 50).

6.3.1. The Storage Relays and their Gates

This description of the storage relays will be given in terms of the constant transmitter cross section drawing PX-11-116. On that drawing there appears a wiring diagram of group one relays, a schematic diagram of group one relays, a coding cam time table, and a cross section of the electronic circuits.

As the IBM card goes through the reader the positions on the card pass under the reading brushes in the following order (see the cam time table PX-11-120 or the small table on PX-11-116).

12, 11, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9,

There are eighty columns on the card and all of these pass under the reading brushes at once. Punches in the ¹¹₄ position will be used to indicate minus signs, while punches in, say, position four represent the digit four in that column.

To simplify the following discussion it will be assumed that leads numbered one to eighty of the Reader connections go directly to the corresponding reading brush. Actually, these eighty connections may be made in any desired manner simply by rewiring the plug-board on the Reader, see PX-11-305.

The relay labeled R_{AB} (schematic diagram of group one relays, PX-11-116) is a PM isolating relay which handles the first three groups (A_L , A_R , and B_L). Referring to PX-11-120 it is seen that cam CB9 makes contact during the reading of the eleven position on the card. If there happens to be an 11 or 12 punch in whatever column the minus indication for group one is placed, say column one, a circuit will be made through connection 97, contact R_{AB} , and the pick-up coils of relays PM_1 and PM_2 . When these relays are picked up they are held by a contact on PM_2 . This holding is controlled

by connection 81 (for group one) and lasts at least (it may last longer, see Section 8.4.5.) until the next card has begun to be read.

The following table gives the various combinations of coding relays that are closed during the various positions of the card reading.

TABLE 8-2

Card position	12	11	0	1	2	3	4	5	6	7	8	9
With no minus indication				C ₁		C ₁		C ₁		C ₁		C ₁
					C ₃	C ₃			C ₃	C ₃	C ₃	C ₃
											C ₅	C ₅
							C ₇	C ₇	C ₇	C ₇	C ₇	C ₇
With minus indication			C ₁		C ₁		C ₁		C ₁		C ₁	
			C ₃	C ₃	C ₃	C ₃			C ₃	C ₃		
			C ₅	C ₅								
			C ₇	C ₇	C ₇	C ₇	C ₇	C ₇				

The reader can check this table in the following manner. If the number is positive the coding relays C₁ to C₈ are connected in pairs to the coding cams CB2, CB4, CB6, and CB8. The coding cam time table shows that as position seven of the card, for example, is under the reading brushes coding cams CB2, CB4, and CB8 are making contact. If seven was punched in the first column storage relays 1-A, 1-B, and 1-D will be activated through the contacts on coding relays C₁, C₃, and C₇. Contacts on the storage relays will cause gate

tubes L'1, K'1, and K'21 to be opened ultimately causing the 1, 2, and 4 pulses (altogether seven pulses) to be transmitted over channel ten. If there had been a minus indication punch the PM relays (PM_1 and PM_2) would be closed (and held by the circuit through connection 81) and the coding relays would be connected to coding cams CB1, CB3, CB5, and CB7. If again, seven were punched in the first column, only cam CB3 is making contact when the seven passes under the reading brushes and the contact on C_3 causes storage relay 1-B to be picked up. Ultimately, this causes the two pulses (complement of seven) to be transmitted over the tenth channel. Since the PM relays are closed, a contact on PM_1 causes gates A'1 and A'21 to be opened. These gates provide (for a five digit number) for the minus indication (nine pulses on the PM channel) and for the correction pulse (to give complements with respect to 10^n).

8.3.2. The Constant and PM Set Switches

PX-11-307 shows that these switches connect directly to the gates for the numbers J_L to K_R . Only the switches for the first and tenth digits are drawn out in detail for the groups J and K. There are four PM switches, so these twenty digits can be used in groups of five and the signs of any one group set independent of the others. If they are to be used for ten digit numbers then both PM switches (J_L and J_R , for example) must be set to P or to M depending upon the number.

The constant set switches consist of four parts mounted on two decks. The moving portion makes contact in such a manner as to open the 1, 2, 2', and 4 gates in various combinations corresponding to the digit to which the switch is set. The gates opened by various switch settings is indicated by the crosses in the following table.

TABLE 8-3a

Gates	Switch Setting									
	0	1	2	3	4	5	6	7	8	9
1		X		X		X		X		X
2			X	X			X	X	X	X
2'									X	X
4					X	X	X	X	X	X

In the case of negative numbers read from cards the coding relays automatically take the complements with respect to $10^n - 1$. This is not true of the constant set switches for groups J_L to K_R , that is, in setting up a negative number on these switches the operator must take the complement himself. No correction pulse is provided by these PM switches so negative numbers are set up as complements with respect to 10^n . The following table illustrates various switch settings.

TABLE 8-3b

Number to be set up	PM Settings		Switch Settings									
	J_L	J_R	1	2	3	4	5	6	7	8	9	10
+23456 on J_L and +78901 on J_R	P	P	2	3	4	5	6	7	8	9	0	1
-12345 on J_L and +78901 on J_R	M	P	8	7	6	5	5	7	8	9	0	1
12345 on J_L and -78901 on J_R	P	M	1	2	3	4	5	2	1	0	9	9
12345 67890 on J_{LR}	P	P	1	2	3	4	5	6	7	8	9	0
-12345 67890 on J_{LR}	M	P	8	7	6	5	4	3	2	1	1	0

8.4. THE IBM READER

The IBM Reader will be described in terms of the wiring diagram FI-11-119. At the top of this drawing are tables which give the locations of the relays and cans. Note that the various parts of one relay (for example, the hold coil, pick-up coil, and various contacts) may be located in widely different places on this drawing. The tables at the top locate all of these parts. The terminal posts are located in the panel behind the motor generator. The connections to the IBM plug (which plugs into a socket on the constant transmitter panel number three) are pictured in the upper right corner of the drawing.

8.4.1. The a-c Circuits

The Reader receives its a-c power by a standard 110 volt plug which plugs into a socket on the bottom of panel three of the constant transmitter. Power is furnished to this plug only when the ENIAC is turned on, plugs at the bottom of other panels, except printer panel #2, have power on them all the time. The a-c power goes through a switch located on the Reader to the motor-generator and through contacts (on H. D. relay at 1A) on a relay (pick-up coil at 2B) to the drive motor. Thus, when the power comes on the motor generator starts up. When it reaches speed the 40 volts d-c cause the green light (on the front of the Reader) to come on and the H. D. relay to close starting the drive motor. The H. D. relay prevents the drive motor from operating in case of failure of the motor generator.

8.4.2. Starting circuits

When cards are initially placed in the magazine, the magazine card lever contact (Mag. at CLC at 2B) is closed. This causes Relay R-1 to pick-up. At this time neither the auxiliary read switch nor the ENIAC starting relay

(in the constant transmitter, see PX-11-307) can cause the reader to operate since Relay 2 is not activated.

If in this case, the initial start key is pushed, the reader will operate, (assuming card stacker switch closed, that is, there are not too many cards in the card stacker) and feed a card into position before continuous roll #1 (that is, in position ready to be read by the control #1 reading brushes). When the card is in position here, relay R-2 is activated by card lever contact #1. Now either the auxiliary read switch or the ENIAC starting relay can cause a card to be read. The initial start switch, since relays R-1 and R-2 are each activated, cannot cause a card to be read at this point. Thus, upon closing either the auxiliary read switch, or the ENIAC starting relay the card passes under the #1 (control) reading brushes and stops in position before the #2 read brushes.

If any of the control arrangements (like plugging to control hubs on the plug-board) are being used the "control" instructions are now remembered by certain relays in the Reader. Note, that this memory depends upon the 40 volt output of the motor-generator on the reader.

With the first card in position before the #2 read brushes, a card lever contact (CLC #1) causes R-60 to be activated. If the auxiliary read switch is again operated this card will be read by the #2 read brushes and the (signed) numbers stored in the constant transmitter relays.

In practice the relay timing is such that in initially placing cards in the reader (by placing cards in the magazine and depressing the initial start key) the reader may feed cards up to position before the #2 read brushes by running through two cycles. In this case it is ready to immediately read the first card. If the first card was fed only into position before the #1 or control

brushes (one cycle) no harm is done. If the reader is now programmed to read, relay R-60 being open, it will read the 1st card by the control brushes and no reset or finish signal will be given out. Then, the starting relay still being closed, the reader will immediately start another cycle in which the first card passes under the #2 brushes. When the cards are in position, relays #1 and #2 are activated by the card contact levers, (Magazine CLC., CR. #1, CR. #2) and the start key becomes ineffective. After relays #1 and #2 are activated, contacts on them (at 3B) enable the auxiliary start key to cause a card to be read. A starting relay located in the constant transmitter (see PX-11-307) has a contact connected in parallel with this auxiliary start key. A unit located in the initiating device (described in 8.2.) causes this starting relay to close and thus causes the reader to read a card.

8.4.3. Numerical Circuits

There are two sets of 80 reading brushes, the first (#1) are the control brushes and the second (#2) are the ones which read the numbers and their signs. The number two reading brushes (at 6B) read the numbers and PM signs on the cards and via connections on the plug board carry the corresponding signals to the storage relays in the following ways:

- (1) Directly to the storage relays (hubs located at 6D).
- (2) For a column in which the PM punch occurs the connection is from the reading brush hub to one of the PM hubs (labeled "minus control" on the plug-board) (at 6D on PX-11-119) and from the other PM hub to the corresponding storage relay hub.
- (3) Or, if desired, the connections from the reading brushes to the storage relays may be by way of the group selector relay contacts (at 6B and 6C). In this manner certain control punches may cause information from one set of reading brushes to go to either

One of two sets of storage relays, or such control punches may cause one set of storage relays to receive information from one of two sets of reading brushes (see Sections 8.4.4. and 8.4.5.)

8.4.4. Group Selection

There are sixteen five-pole, double-throw relay switches (relays R24 to R55, two relays to each switch, hold coils at 4C and 5C, contacts at 6B and 6C). The coils at 4C and 5C serve for picking up and for holding. These five-pole, double-throw switches may be used to rearrange the information coming into the storage relays. These relays are picked up by contacts on relays 7 to 22 (at 4C and 5C) in series with the cam P6. Once they are picked up they are held by cam P7.

Referring to the cam time table (PX-11-12C) we see that relays 7 to 22 may be picked up any place in the card cycle, that is, from any punch (since cam P5 makes contact all this time). If any of these relays have picked up, cam P6 will cause the corresponding relays 24 to 55 to pickup at the end of the card cycle. Once they are picked up cam P7 holds them until the end of the next card cycle. Since the card going under the control brushes will go under #2 read brushes exactly one card cycle later, this means that a group selection control punch will activate the group selection relays during the time the card is passing under the #2 read brushes.

8.4.5. Reset Control and Reset Shunt

The storage holding relays (contacts at 7B, pick up coils at 3C) 4, 5, and 6 cause the relays in the constant transmitter to hold their information. The time table shows that cam CB10 causes these relays to hold from position 12 on one card until 13.7 on the next card. That is, the information read from one card is normally dropped out at the beginning of the reading of the next card.

By plugging from the reset control hubs to the reset shunt the corresponding constant transmitter relays can be caused to hold their information until such time as the relays 56 to 58 are activated.

By proper plugging on the plug board connection can be made from the #1 read brushes through the pick up coil of relay 23 to the digit selector. When relay 23 is activated relays 56 to 58 will be picked up by cam P8 at 8.5 in the card cycle. A contact on relay 57 and cam P1 causes relay 59 to pick up at 9.5 in the card cycle. This is shown on P-11-306.

Suppose that reset control is operated from a "three" punch in some column in what will be called a master card. Cards without this "three" punch (in that same column) will be called detail cards.

At the end of a cycle in which such a master card passed under the control (#1) brushes relays 23, 56 to 58, and 59 have all picked up. During the next card cycle the master card will pass under the #2 read brushes. Relay 59 holds until near the end of this cycle preventing either a reset or a finish signal. Inspection of the reader starting circuit on PX-11-307 shows that the starting flip-flop (65,66) is still set and that the starting relay is still activated so the reader immediately goes on to read another card. The relays which are shunted (by plugging reset control to reset shunt on the plug board) will hold the information read from the master card until another master card comes along. New information will be put into the other relays for each detail card.

8.4.6. Coding Cams

The coding cams are located at 6A and 7A on PX-11-119. They directly operate the coding relays located in the constant transmitter. See 8.3.1.

8.4.7. Reset Signal

Cam P4 produces the reset signal at time 12 in the card cycle. This signal will be sent to the constant transmitter (actually to the initiating unit) only if relay 60 is activated and relay 59 is not. Relay 60 is activated only when cards are in position at the #2 read brushes (see CR#2 at 3B, that is, continuous roll #2). Relay 59 is activated only when a "master" card (a card with a punch operating reset control relay 23) is at the #2 read brushes.

8.4.8. Finish Signal

Cam P3 produces the finish signal at time 9.5 in the card reading cycle. As with the reset signal this signal is obtained only if relay 60 is activated and relay 59 is not.

IX. PRINTER AND IBM GANG PUNCH

The printer causes eighty digits and as many as sixteen PM signs which are stored in certain accumulators and possibly the master programmer to be punched on IBM cards. In the case of complements (which represent negative numbers) the printer relays cause the IBM punch to punch the true negative number and a corresponding sign indication (an 11 punch).

When operating continuously the IBM punch can punch a card in 0.61 seconds. However when starting from rest, the inertia of the punching mechanism makes the punching time 0.82 seconds. The units of the ENLAC associated with the printer (eight accumulators, say, and five decades of the M.P. do not have to wait while the complete punching cycle takes place but only 0.4 seconds. If the punch is programmed before the end of the first cycle to punch a second card then the two cards will be punched in 1.4 seconds. However, if the second program signal comes anytime after the first cycle is completed the punch essentially loses a cycle (because of the clutch **dropping** out) and the punching of two cards will take at least 2.0 seconds.

Therefore, if there is no more than approximately 2,000 addition times between printing programs, the punch will punch almost 100 cards per minute. A small increase in the number of addition times between printing programs will cut this down to not more than 50 cards per minute. It should be emphasized that while all these figures are valid at the time of writing, they may vary with time, temperature, punch wear, and so forth.

The program control circuits for the printer are located in the initiating unit. When programmed to print, the IBM punch will start, the

relays in the printer will be set up by the static outputs of the various decades and PM units, a reset signal will come from the punch to the program control circuit, and the punch will complete the punching cycle. The reset signal can be used to continue computation in the ENIAC. Since the set up time of the relays is small compared to the time for punching a card this arrangement prevents undue waste of time while the card is being punched. When the card punching cycle is completed an interlock signal comes from the punch to the printer allowing the relays to set up anew provided another print program signal came along in the meantime. This constitutes a mechanical interlock arrangement.

On the printer there are sixteen "print" switches which enable the operator to print or not print any one of sixteen groups of five digit numbers and the associated PM indication. There are sixteen coupling switches which make possible the printing of groups with ten or more digits. These coupling switches serve no purpose when printing positive numbers. In printing negative numbers they take care of the carry over in the process of taking the complements and also gang the PM relays for the coupled groups.

The description of the printer will be given in terms of the following drawings:

Printer Cross Section	PX-12-115
Printer Block Diagram	PX-12-307
IBM Gang Punch	PX-12-112

The discussion will be divided up in the following manner: 9.1, Program Control Circuits, 9.2, Numerical Circuits of the Printer, 9.3, IBM Gang Punch, and 9.4, Examples.

9.1 PROGRAM CONTROL CIRCUITS

The printer program control circuits comprise most of two plug-in units in the initiating device (PX-9-104 and PX-9-105) and the printing switches located on panel two of the printer. The circuits located in the initiating device are represented in block diagram form on PX-12-307 (lower left corner) or PX-9-30, and in detail on PX-12-115.

9.1.1 The Printing Switches

The printing switches simply disconnect the power (+200 v line) to the digit and PM relays of each group. Thus, if the print switch for a particular group is set at "off", the relays of that group cannot pick-up and thus nothing will be punched in the corresponding position on the card.

9.1.2 Starting Circuit

Any pulse arriving at the printer program input terminal P₁ (see PX-9-302) will (through the buffer 67) set the flip-flop (68 and 69). This causes the driver 70 (which has its cathode at +20 volts, and has the starting relay as its load) to come on, closing the starting relay (located in the printer panel No. 3). This flip-flop will be reset by a signal arriving from the punch through the buffer 72. (It can be reset by an ICG, see Section 9.1.5.)

9.1.3 Reset and Program Output

After the printer relays have set up, (these relays set up when the interlock can makes contact and the starting relay is activated) near the beginning of the card punching cycle (at card time 11.2) the reset signal will arrive at the printer from the punch. This signal passes through the special pulse standardizer 61 and 62 (in unit PX-9-105, see PX-12-307; for a description of this circuit see Section 1.2.7). The

output of this pulse standardizer sets the flip-flop 64 and 65 and also through the inverters 63 provides a reset signal for the starting flip-flop described above.

The flip-flop 64 and 65 opens the gate 66 passing a CPP which sets the flip-flop 67 and 68. The output of this flip-flop gates a CPP (gate 69) which resets the two flip-flops passing through the transmitter 70 to 72, and appears at the printer output terminal P_0 on the initiating unit front panel (see PX-9-302). At the time of writing this report, starting with the punch at rest about 1900 addition times elapsed between a reception of a program pulse at P_1 and the output program from P_0 . This time will probably vary with respect to temperature and age of the machine among other things.

This double flip-flop arrangement is a synchronizing device. Since the timing of the reset pulse depends upon the mechanical operation of the punch it will generally not be synchronized with the CPP in the LC. The output of the gate 66 will be synchronized, but it cannot be transmitted since the flip-flop 64-65 may be set at such a time that it could pass a substandard pulse. If the CPP passed by 66 is weak and does not set the flip-flop 67-68 no harm is done for the next CPP (64-65 is reset in this case) will be standard and will set 67-68. The circuits comprising these flip-flops and their associated gate tubes are relatively slow (the rise time is on the order of 50 μ seconds). Thus, if a CPP sets flip-flop 67-68, the gate 69 will open only in time to safely pass the pulse which arrives one addition time later, and the output of gate 69 will always be a standard pulse. Note that this program output occurs before each punching cycle is completed (assuming the punch starts from rest

and at the time of writing this report this time was approximately 1950 addition times).

9.1.4 The Interlock Cam

The interlock cam makes contact near the end of the punching cycle (card time 13.3) and breaks near the PFI punch of the next card cycle (time 12.8) (see the time table on PX-12-307). This cam and a contact on the starting relay (in series) connect the cathodes of all the tubes in the printer to +20 volts. When this circuit is open the cathodes rise (see the 2K, 10 watt resistor near the starting relay on PX-12-307) to about 200 volts. Since this is about the same potential as the plates, any signal on the grids (and generally there will be signals on certain of the static outputs) will not cause any of the tubes to go on and set up their corresponding relays.

The printer may again be programmed to print any time after the reset signal has arrived (see Section 9.1.3). However, except for the activation of the starting relay, nothing will happen until the end of the cycle which the punch is in; until the interlock cam makes contact. This furnishes a mechanical interlock arrangement. The second print signal cannot cause any tubes to conduct and relays to set up in the printer until the first punching cycle is complete. At time 9.5 in the first cycle, the holding cam breaks contact releasing all relays in the printer. At time 13.3 the interlock cam makes and (provided the start relay is activated) the printer relays set up in the new way and a second card is punched.

Table 9-1 gives the timing of the printing sequence.

TABLE 9-1

Mn. Time lines secs.	Card Time	Activity
0 0	D	Printer program pulse arrives (at initiating unit). Starting relay closes (in printer). IBM punch starts and relays set up.
	13.6	Carry-over cam makes
	14.5	Holding cam makes.
	12.8	Interlock cam breaks (this turns off all tubes in printer and, thus, releases the accumulators and master programmer for other activities).
	11	PM indications are punched.
1900 to 2000	11.2	Reset cam closes causing 1) Starting flip-flop to reset 2) Printer program output pulse to be transmitted. ENIAC proceeds with other computing
	11.8	Reset cam breaks.
	0	
	1 to 9	Digits are punched.
	9.36	Carry-over cam breaks.
	9.45	Holding cam breaks
050 .6	13.3	Interlock cam makes. Relays will set-up again as soon as starting relay is closed. Note that the next printing signal may arrive any time after the reset cam breaks, that is, any time <u>after</u> 11.5.
	D	Punch stops unless starting relay has been closed.

Clearly, the programming in the ENIAC must not be arranged so that a second print program input pulse arrives at P_1 before the reset signal has been given out by the punch and the flip-flop 68-69 has been reset. Hence, no pulse should be supplied to the printer program input until after a pulse has been omitted from the printer program output P_0 . Any pulse arriving after the reset signal but before the end of the card punching cycle (that is, during the period 11.2 to D) will be remembered and will cause the punch to continue and punch the next card.

9.1.5 Initial Clear

The only place that the initial clear gate is used in the printer circuits is to reset the starting flip-flop 68-69 (PX-9-104 in the initiating unit). The characteristics of the tubes in these circuits are such that whenever the power is turned off or turned on (in spite of the automatic initial clear) the starting relay will be closed long enough to cause the punch to feed a card through.

9.2 THE NUMERICAL CIRCUITS OF THE PRINTER

Of the sixteen relay groups, groups one and sixteen and parts of groups two and fifteen are represented on PX-12-307. Assume that the plug-board is so wired that the columns (A, B, C, D, and E) correspond to the first five columns on the IBM card. Suppose, furthermore, that the PM indication for this five digit group is to be punched in column one or A.

There are fifty digit triodes in group one (actually 25 6SN7's) and three PM triodes. The grids of these tubes connect directly by a 51 line cable to the static outputs of the decades and PM unit of an accumulator. Just one PM line goes to the three grids of the PM tubes.

The tubes in each column are denoted by A0 to A9, B0 to B9, et cetera; that is, the second symbol denotes the digit represented by that tube being on. The grids of these tubes are connected to the normally negative outputs of the stages of the decade rings. The PM line in the cable goes to all three PM tubes (the tubes driving the carry-over relay C_0 , and the PM relays M_1 and M_2).

The leads from the emitter arrive at the upper left corner of PL12-307. These emitter leads go through transfer contacts on the relays M_1 and M_2 to the various digit levels in the five columns of relays.

All the digit and PM relays have holding contacts connecting them to a line controlled by the holding cam. The holding cam makes at the beginning of the punch cycle (at IBM time 14.5, see Table 9-1) and breaks at the end of the cycle (at 9.45). These holding contacts cause any relays which are picked up by tubes conducting to remain up until the end of the cycle. Thus, the printer tubes need to conduct only long enough to safely pick up the relays. This determines the length of contact made by the interlock cam (13.3 to 12.8) (note that if the punch stops between cycles then the tubes begin to conduct at time D = 13.5 when the starting relay is activated). Once the relays are picked up the tubes can be turned off by the interlock cam and all the units which connect statically to the printer groups whose print switch is "on" can then be released to participate in further computations.

If the interlock cam has made contact and the starting relay is closed, then one digit relay (in each column) picks up, corresponding to the actual number registered in the decade of the accumulator or master Programmer. All three PM relays will pick up together if the number is negative.

Suppose the number 112345 is registered in the decades and PM unit of an accumulator associated with group one relays. If the print switch of group one is set to print and the starting relay is closed (assuming the interlock cam is making contact) then the tubes A1, B2, C3, D4 and E5 will conduct closing relays A1, ..., E5.

As the card passes under the punches, pulses arrive from the emitter over the emitter lines. Since the above number was positive all three PM relays (C_0 , M_1 and M_2) are unactivated. This means that there is a connection from emitter line "one" through the transfer contact on I1, through the contact on A1 to the transfer contact on C1, and on to the punch magnet (via the punch plug board) for column one on the card. Thus, when the one position on the card is under the first column punch a signal from emitter line "one" will (through this circuit) cause "one" to be punched in the first column of the card. The circuits for the above number and for 112378 are illustrated by the rows in the following tables.

In these tables (A) denotes that the relay is in the abnormal or activated position while (N) means that the relay is in the normal position.

The resistance-capacitance circuits found on the contacts of the carry over relays (and on one contact of the starting relay) are to prevent arcing at the contacts. The protection is necessary only on contacts which carry relative heavy loads, and not only prolongs the life of the relay but provides more reliable operation.

In the case of the number 112370, the minus indication will cause relay C_0 to be activated which in turn (assuming the coupling switch 1-2 is set to "0") causes C_5 to operate. Since the last digit is zero, relay E0 (group 1 relays) will be activated which will cause C_4 to operate.

TABLE 9-2

Circuits For The Number P12378

Emitter Line	PI relay transfer contact	Digit relay contact	Carry-over relay transfer contact	Line to punch magnet (via plug-board)
1	M1 (N)	A1	C ₁ (N)	1
2	M1 (N)	B2	C ₂ (N)	2
3	M1 (N)	C3	C ₃ (N)	3
7	M2 (N)	D7	C ₄ (N)	4
8	M2 (N)	E8	C ₅ (N)	5

TABLE 9-3

Circuits For The Number M12378 (-87622)

(Relays C₀, C₅, M₁, and M₂ are now activated, C₁ to C₄ normal, Coupling Switch at 0.)

Emitter Line	PI relay transfer contact	Digit relay contact	Carry-over relay transfer contact	Line to punch magnet (via plug-board)
8	M ₁ (A)	A1	C ₁ (N)	1
7	M ₁ (A)	B2	C ₂ (N)	2
6	M ₁ (A)	C3	C ₃ (N)	3
2	M ₂ (A)	D7	C ₄ (N)	4
2	M ₂ (A)	E8	C ₅ (A)	5

Note: In the above tables (N) means the relay is in normal or unactivated position while (A) means it is in the abnormal or activated position.

The carry relays C_1 , C_2 and C_3 will not be activated so the circuits take complements with respect to ten (modulo ten) in the units and tens place and with respect to nine in the other places.

It is essential that the carry over cam breaks before the holding cam does. If the holding cam were to break first, then a string of carry over relays which may have picked up would be dropped by the contact on relay C_0 and since the carry over relays which have picked up are connected in parallel the load here would soon burn up the contact on C_0 . Since the carry over cam breaks first (at 9.36 as against 5.45 for the holding cam) the contact on C_0 will not be breaking any current.

There is one PI unit in each accumulator and there are two sets of PI relays (one set with each five digit group). Thus, to print ten digit negative numbers the PI static output must be connected to both sets of PI tubes. This is accomplished by the use of an adapter which connects the two PI lines to the one static output. In case of twenty digit operation an adapter must be used to connect the four sets of PI tubes to the PI static output of the left hand accumulator.

The adapters for the ten digit operation are installed in the backs of the respective accumulators. This adapter (see PX-12-114A) is a plug and two sockets; the plug goes into the PI static socket (on the PI-clear plug-in unit) and the two sockets receive the two PI lines of the two static cables. The adapters for more than ten digit operation are best installed in the printer (behind front panel No. 2) (those for ten digit operation could be installed here, too).

To make it possible to print the actual numbers registered in certain decades (regardless of sign) there is a ground lug on the printer

plugs which normally connect to the static P1 leads. Another adapter (a socket with a jumper inside, see PX-12-114B) used here grounds the grids of the 6X tubes. This prevents them from conducting; if the grids are allowed to "float" the tubes may or may not conduct. Such an adapter must be used, for example, whenever printing numbers from decades in the master programmer.

9.3 THE IBM GANG PUNCH

The IBM gang punch will be described in terms of diagram PX-12-112. This punch was constructed in the following manner: An unfinished standard gang summary punch was removed from the assembly line and certain details, such as cams and column split relays were added to make a punch for use with the ENIAC. This means there is some unused apparatus in the punch; for example, there is a set of control reading brushes and the continuous roller is in for the regular set of reading brushes. This also explains why there are shunts on some relay contacts. The master-detail switch located on the front of the punch simply acts as an on-off switch for the punch magnets ("on" corresponds to "master").

9.3.1 The a-c Circuit

The a-c connection is normally plugged to the outlet on the bottom of panel two of the printer. Power is furnished to this outlet only when the ENIAC is turned on. Outlets on all other panels except panel three of the constant transmitter have power all the time. Thus, if it is desired to operate the punch without turning on the ENIAC one of the outlets of one of the other printer panels may be used.

When the a-c power is turned on K.D. relays No. 2 and No. 3 close starting the motor generator and closing the 40 volt d-c circuit. The

green light on the front of the punch indicates that the motor generator is operating properly. The drive motor is started by the closing of contacts on R.D. relay No. 1. The pick up coil for this relay is in parallel with R9. R9 is picked up by a contact on R10 and another contact on R10 operates the clutch. Thus, relay 10 is the starting relay.

9.3.2 The Starting Circuit

There are three card lever contacts,

- 1) Die card lever contact (Die CLC)
- 2) Magazine card lever contact (Mag. CLC)
- 3) Brush card lever contact (Br. CLC)

which activate relays 1, 3, and 7. These card lever contacts determine if the cards are being fed in properly. There is a die contact which determines if the punch die is in proper position. If the die contact is open, neither the start key on the punch, nor the starting circuits of the ENIAC will operate the punch. The various card lever contacts are bypassed by the start key on the punch. Thus, it can be used to feed the cards into position when they are first put into the magazine.

If the magazine runs out of cards the punch will stop. If the starting relay is closed the printer relays will pick up and the punch will operate the moment new cards are placed in the magazine. The operator should hold down the stop key when putting new cards in this case. Otherwise, the punch may start before the cards are firmly seated and may fail to feed the first card.

To start the punch, the ENIAC completes the circuit from terminals one to eleven. This, through contacts on relays 1 and 3, closes R23. A contact on R23 causes R10 to close. Contacts on R10 cause R9, relay

H.D. No. 1, and the clutch to pick up. Relay 9 and H.D. relay No. 1 are held by R10 and by the continuously running cam (C.R. cam). Relay 10 in turn is held by cam P5. Thus, when the starting relay is closed in the printer, relays 9 and 10 pick up and hold until the end of the card punching cycle. At that time they drop out as does H.D. No. 1. The clutch drops out when relay 10 drops and the drive motor coasts to a stop.

Note that the operator must use the initial start switch to feed cards into position when starting, since with cards only in the magazine, the ENIAC starting circuits will not operate.

A card stacker switch opens the starting circuit when too many cards are in the stacker. When the cards are removed the machine will continue to operate in the proper manner.

9.3.3 The Column Splits (PL Circuits)

The pick-up coils of the column split relays are located at 5C on PL-12-112. These relays are activated by cam P2 during the time that the 11 and 12 positions of the card are passing under the punches (actually, from 13.5 until 11.6). The relays act as a sixteen-pole, double-throw switch (see the contacts at 7 and 8 A and B) and connect the punches (via plug-board connections) to the minus indication terminals (at 8D) during the 11 and 12 positions of the card and to the computer result exit terminals (8D) during the rest of the card cycle. This makes it possible to punch a P. indication and a digit of a number in the same column.

9.3.4 The Punch Magnets

The circuits to the punch magnets is completed by contacts on relays 43 to 56. These relays are activated by a circuit through the

master-detail switch (with switch setting on "master"), a normally closed contact on R14, and cam P12 (makes at 14.3 and breaks at 9.3).

9.3.5 The Dnitter

The emitter is located at 100. It turns in synchronism as the card passes under the punch magnets, that is, the emitter connects to line 3, for example, when position three is under the punches. If the circuit is completed from emitter line three back to the punch magnets then three will be punched.

9.3.6 The Plug-board

Instructions for plug-board connections appear on FX-12-305. The eighty-digit outputs appear on eighty hubs on the plug-board. The eighty punch magnets appear on eighty other hubs. Thus, information can be rearranged on the card in any desired manner.

X. MASTER PROGRAMMER

The master programmer occupies two panels. The two panels are practically identical in function and in appearance. The Block diagram PX-8-304 refers to the left hand panel; however, by changing some of the terminology, it can refer equally well to the right hand panel. Thus, in the following discussion only the left hand panel will be considered. In the left hand panel the decades are numbered from 11 to 20 (reading from right to left as in an accumulator) and the steppers are named A, B, C, D, and E (from left to right). In the right hand panel the decades are numbered from 1 to 10 and the steppers are named F, G, H, J, and K.

10.1. INTRODUCTION.

The Master Programmer contains only program circuits, there being no numerical or common programming circuits. The program circuits will be divided into two types, namely, stepper circuits and decade counter circuits or decade units. The decade counter circuits are represented on PX-8-304 by the ten rectangles along the top of the drawing. The five steppers are represented by the rectangles along the bottom. The decade counter circuits are divided into groups, each group being associated with a stepper. To give flexibility decade associator switches are provided which change a decade circuit from one group to another.

10.2. DECADE COUNTER CIRCUITS.

10.2.1. Decade ring. The decade rings used in the master programmer are ten

stage ring counters located on plug-in units. The clear inverter (tube 1) is also located on the same plug-in unit. The pulse standardizer and the carry circuits associated with the ring are on a separate plug-in unit. In fact, for each pair of decades the pulse standardizers (21-23 and 25-27) and carry circuits (24, 28-31) are on one plug-in unit.

Provision is made for making static cable connections to any decade ring of the master programmer. This would enable the operator, for example, to register an independent variable in certain decades of the master programmer and to print it whenever desired.

The normally positive outputs of the stages of the decade ring go to the respective positions on the six decade switches. The common connection of each switch connects to the grid of the inverter tube B 41-43 for decade 11). If there is a coincidence between the setting of any decade switch and the position of the decade ring the corresponding inverter will be turned off. Since all the switches are illustrated as setting at "7" all the inverters would be turned off if the decade ring was stepped to stage seven.

The carry circuit. Whenever a decade is stepped to stage "nine" the static output causes gate 28 to open. If another pulse is fed into the pulse standardizer the ring will step to zero and a pulse will pass gate 28 (or gate 24 for even numbered decades), go through the inverter and buffer 30 and thence to an association switch or, in some cases, directly to the input of the pulse standardizer for the next decade to the left.

The carry circuit is spread over parts of three plug-in units and, thus, necessarily has a very poor time constant. Actually, the rise time for

the circuit comprised of stage nine of the ring and gate 28 on a separate plug-in unit (four times the time constant) - approximately the time for the signal to reach 97% of its maximum amplitude is on the order of one-half an addition time. Thus, any sequence of digit pulses which would produce a carry-over cannot be fed into the decades of a master programmer during any one addition time. There are other situations (see the discussion of clear circuits below) where digit pulses cannot be fed into these decades.

The clear circuits. This ring is cleared by a CPP passing gate B44, for example, and turning off the clear inverter (tube 1) on the decade plug-in unit). This clear circuit is operated either by the initial clear gate arriving at the buffer B45, say, or by the operation of one of the coincidence gates (B, C, 48-50) in the stepper circuits (E). Generally, one of these coincidence gates will conduct when there is a coincidence between the position of the stepper ring, the settings of a number of decade switches and the position of the corresponding decade rings.

Since the clearing is accomplished by a CPP passing gate B44 (in decade 11) the decade cannot be stepped by any number of digit pulses (arriving over the direct input 11di) which will step it past a coincidence position. This restriction is not because of the time constants. Actually, for the clearing to take place the ring must come to (and stay on) the coincidence position (that is, the position corresponding to one of the decade switch settings) so that gate 63 is set up at pulse time 17; and pulse time 17 is some time (at least seven pulse times) after the last digit pulse arrived. In fact.

digit pulses should not be used to step this ring to a coincidence position. The rise time of this clearing circuit, (as well as the stepper clear circuits) is on the order of one-half an addition time (10 pulse times). Thus, the circuit can be expected to operate satisfactorily only when stepped to the coincidence position with a program pulse (CPP). Note that the time constant of these circuits vary considerably depending upon the positions of the association switches and the stepper considered.

Note that there is no provision for delayed carry-over (as in an accumulator). This means that two associated decades cannot be stepped simultaneously in a manner which produces a carry-over.

10.3. THE STEPPER CIRCUITS.

10.3.1. The stepper ring. The stepper contains a six stage ring located on a plug-in unit. On the same plug-in unit is a pulse standardizer and a set of inverter tubes connected to the outputs of the ring. All of these circuits use the tubes numbered from 21 to 32. The set of outputs of the ring which go through the inverters go to two sets of six gates each, B and C 48 to 50 and the gates numbered 61, 65, and 69. The other outputs of the stages of the ring go to the respective positions on the stepper clear switch. The common terminal of this switch goes to gate B47. When B47 is open any pulse arriving from the inverter 61 and buffer 62 will clear the stepper back to stage one. The stepper will clear to stage one in the following cases:

- a) When the initial clear gate is applied, gate C47 opens letting through a CPP1 which turns the inverter C46 off clearing the ring.
- b) A pulse arriving over the clear direct input (cdi) turns the

buffer B46 on and the inverter C46 off.

c) If the stepper is set at stage five and the stepper clear switch is at five (as illustrated) the gate B47 will be open. A pulse passed by gate 63 or from the buffer 61 on the stepper direct input (di) will turn the inverter 61 off and the buffer 62 on. This will cause the inverter B46 to go off causing the gate tube B47 to conduct. This in turn causes the clear inverter C46 to go off and clear the ring.

The stepper clear circuit. The stepper clear circuits will not operate in one pulse time (the rise time for this clear circuit is about one half an addition time).. This means that the stepper ring can be stepped with digit pulses only if the ring is not stepped onto the coincidence position (that is, onto the stage corresponding to the setting of the stepper clear switch).

The stepper direct input. A direct input (through buffer 61) is provided to step the stepper ring. In this case the associated decade units ring is not stepped and no output program pulse is obtained. Note (above) the restrictions on the kinds of pulses supplied to this input.

The stepper input. The flip-flop (66,67) and the associated gate 69 has a time constant approximately equal to that of the slow buffer output of a transceiver. This means that this input (E_1 for example) must never be pulsed later than pulse time four. That is, it can be pulsed by a CPP, 9P, 1P, 2P, or 2'P; but not by 4P, 1'P, or generally by any digit output of an accumulator.

Note that if E_1 and E_{cdi} , for example, are pulsed simultaneously, the stepper will clear first and the output pulse will be from E_{1c} .

2.3.2. The program transmitters.

In the lower right hand corner of the rectangle (PX-8-304) containing the stepper circuits there are six gates and six standard transmitters. One of these gates will be open depending upon the position of the stepper ring. Any pulses arriving from the buffer 70 will be transmitted through one of these channels. In the illustration the stepper is setting at stage one so any pulses from 70 will be transmitted through the left hand gate 61 and will appear on the output terminal E_{10} . Note that a lead comes from the master programmer clear (MPC) to all these gate tubes. Inspection of the cross section PX-8-102 shows that this lead goes to the screens of these gate tubes (6SA7's). Whenever the initial clear is activated a relay located in the initiating unit changes these screen voltages from +150 to 0 volts. This blocks these gates, that is, even if a signal arrives on both control grids the tube will not conduct. As explained in section 2.1.2. the effect of the initial clear is to clear decades back to their first stages and let the program circuits run out their sequences. By program jumpers various program controls in the machine may be connected in a sequence that will take several hundred addition times to run out. These sequences may be tied together by the master programmer so they would take a very long time to run themselves out or even repeat indefinitely. To prevent this tying together and, thus, make the time for initial clearing reasonably short the output gates in the master programmer are blocked in this manner. A period of about one half second will be sufficient (including a safety factor) for any possible sequence set up in the other units of the ENIAC to run out, therefore, the initial clear lasts for approximately one half second.

10.3.3. The program receiving circuit.

The input program will ordinarily come in by the terminal Ei causing the buffer 65 to go on setting the flip-flop 66 and 67. The output then takes a positive swing opening gate 69. The next CPP is passed resetting the flip-flop and turning off the inverter 68. This causes the cathode follower 70 to go on giving a positive pulse to the grids of the gates 61, 65, and 69. This also turns the buffer A43 on giving a negative pulse to the pulse standardizer of decade 11.

As described above, 10.3.2, one of the six gates (61, 65, 69) is open depending upon the position of the stepper. Thus, for every pulse put into Ei a pulse is sent into decade 11 and a pulse comes out of one of the terminals E_1 to E_6 . one addition time later.

Pulses fed into Edi cause the stepper to step, and pulses fed into 11di cause the decade to step. Neither of these cause any pulses to be given out at the outputs E_1 to E_6 .

10.3.4. The coincidence gates.

The coincidence gates are the tubes B and C 48 to 50 for stepper E. Whenever any one of these gets a signal on both grids the inverter 64 goes off and the gate 63 is opened. This passes the next CPP to the inverter 61 and the buffer 62. The output of 62 goes to the pulse standardizer 21, 22, and 23. stepping the ring and it also turns the inverter B46 off. If the gate B47 is open the clear signal from C46 safely overrides the stepping signal from the pulse standardizer and the ring clears back to stage one. Also, a pulse on the clear direct input (edi, B46) or a CPP passed by gate C47 (when initial clear is activated, will safely (that is with adequate safety factor) override any stepping signal.

The output of the stepping gates also goes to the clear circuits in the decade counter causing the decade to clear back to zero. Again, this clear signal overrides any stepping signal.

Stepper E, with the decade associator switch for decade 12 setting as illustrated, has only one decade associated with it. Consider stepper D. This stepper has decades 12 and 13 associated with it. Looking at stepping gate E48 it is seen that one of the grids connects to both the inverter D41 and through the D-E associator switch, to the inverter C41. If either inverter is conducting the grid on E48 will be sufficiently negative to prevent it from conducting. This constitutes a multiple coincidence arrangement. That is, in order for E48 to conduct three inverters must go off, namely, C41, D41, and X in the stepper ring unit. Consider stepper C. If five decades are associated with stepper C then in order for the stepping gate G48 to conduct the inverter in the stepper ring unit must go off along with the five inverters in the respective decade units.

Steppers A and F may be used without any associated decades. When the A-B association switch (or the F-G) sets at B the screens of the coincidence gates (L, K, 48-50) are switches from +150 to 0 volts. This prevents any of these gates from conducting and, thus, gate 63 never conducts. This means that the stepper ring can be stepped only by pulses introduced over the direct input. The stepper clear direct input functions as before. Any pulses arriving over the program input will be transmitted over one of the six outputs depending upon the position of the stepper ring.

Any of the other steppers may be made to operate in the above manner by removing the gate 63 in the plug-in unit. Note, that the only difference

in the operation of these other steppers (as compared to A or E) is that certain decades will count the pulses coming in on the stepper program input. These decades will clear at positions depending upon the settings of the decade switches but there will be no corresponding change in the stepper position. This clearing could be prevented and, thus, the total number of program pulses counted by removing the coincidence gates (D, E, 48-50, for example) instead of gate 63.

10.4. ASSOCIATION SWITCHING.

All the decade units are exactly alike, and the stepper units only differ with respect to the number of decades that can be associated with each one. PI-8-304 shows that decade 12 can be associated with either stepper D or E. Decade 14 can be associated with either C or D, decade 18 with either B or C, and decade 20 with either A or B. When decade 20 is associated with stepper B then stepper A has no associated decade (see above).

The decade associator switch is a nine pole double throw switch. The six poles on the left handle the outputs of the inverters associated with the decade switches. The seventh pole takes care of the clear circuit, the eighth the input to the next decade on the left, and the ninth the input of the decade to be associated. In the case of decade 20, since there is no decade to the left, the eighth pole takes care of the input to decade 20, and the ninth pole is used to change the screen bias of the coincidence gates.

Consider the associator switch for decade 12. As illustrated this decade is associated with stepper D. The following table illustrates what happens for the two positions of the associator switch for decade 12:

TABLE 10 - 1

	Associated with D	Associated with E
Outputs of the inverters C41 to C43	Go to stepping gates E and D 48 to 50.	Go to stepping gates B and C 48 to 50.
Decade clear input (to C45)	Goes to the output of the stepping gates E and D 48 to 50.	Goes to the output of the stepping gates B and C 48 to 50.
Input to decade 13	Goes to the carry over circuit of decade 12.	Goes to the buffer AAA of stepper D.
Input to decade 12	Goes to the buffer AAA of stepper D.	Goes to the carry over circuit of decade 11.

Thus, when decade 12 is associated with stepper E, decade 11 acts as a units decade and 12 as a tens decade in counting the number of program pulses coming in at the terminal E₁. Therefore, the two decades can count as many as 99 pulses coming in at E₁. When decade 12 is associated with stepper decade 11 acts as a units decade in counting the number of pulses coming in at E₁ and cannot count more than 9 pulses. In this case decade 12 acts as a units decade in counting the number of pulses coming in at D₁.

Consider stepper C. If both decades 14 and 18 are associated with stepper C then the five decades (14 to 18) can count as many as 99,999 pulses arriving at terminal C₁.

XI. THE TRANSMISSION SYSTEM AND SPECIAL DEVICES

This chapter contains a description of the digit and program trunks which carry the pulses representing digits or program signals from one unit to another. Also various special devices such as shifters, deleters, adapters, static cables, and so on, are described in this chapter.

11.1 TRAYS AND TRUNKS

It is necessary to transmit pulses representing digits or program signals from one unit of the ENIAC to another. Furthermore, this must be done in an entirely different manner for each new problem that is put on the ENIAC. Thus, the interconnection systems must be very flexible. For this purpose trays and jumpers are used.

11.1.1 Trays

A tray is essentially an eleven wire transmission line, capable of being connected to other trays and to the digit terminals and program terminals of the various units.

Each tray is eight feet long, nine inches wide, one and a quarter inches deep, and open at the bottom. It contains eleven wires separated from each other by metal shields. The trays are placed on top of one another so that they will actually be shielded on all sides. Each tray is equipped with outlets on each end so that it may be connected to other trays by means of jumpers. It also has outlets every two feet of its length so that it may be connected to the program and digit terminals of the various units of the ENIAC. These outlets are of two kinds:

A digit tray, - shown in drawing PX-4-29, has for each outlet a twelve-contact plug (eleven wires and ground).

A program tray, - shown in PX-4-101, has for each outlet a set of eleven two-terminal plugs (one wire and ground). At each end of the program tray is a twelve contact plug to facilitate its connection by a jumper to another program tray.

These trays are stacked on the front of the various units of the ENLAC, some above and some below the program control panels. Generally, the program trays will be placed below the control panels and the digit trays will be placed above. There is room for about twelve trays to fit above and twelve below the control panel of a unit, although a much smaller number will ordinarily be sufficient.

11.1.2 Jumpers

Cables or jumpers are used to connect the trays to the digit terminals and program terminals. There are two kinds of jumpers. One, a program jumper, consists of a single wire and ground and is used to connect a socket on a program tray to a program socket on one of the units. The other, a digit jumper, has eleven wires and a ground and is used to connect an outlet on a digit tray to a digit terminal of a unit. This last type of jumper is also used to connect trays together.

11.1.3 Trunks and Lines

A single wire and ground, running through several program trays, jumpers or program cables and thus connecting a number of program terminals to one another, is called a program line. A set of eleven wires and ground used to transmit a ten-digit number and its sign and running through several digit trays, jumpers or cables, is called a digit trunk.

One set of digit trays (9) are connected together to form the cycling unit trunk. This carries the various pulses and gates produced by the cycling unit around to the various units of the ENIAC. Nine trays are sufficient here since the printer does not connect to this trunk. See PL-9-307.

11.1.4 Load Boxes

Each wire of a digit trunk and each program line has one load resistor connected to it. These resistors are assembled in boxes, (see PL-4-103) and one box is to be plugged into an otherwise unused outlet at the end of one of the end trays of each set connected together by jumpers. As explained in Section 1.2.8, this makes it possible to have the flexibility of being able to connect varying numbers of digit and program terminals to the trunks and program lines.

11.1.5 Load Units

The pulses and gates transmitted over the trays must have rise times better than $1/2$ microseconds. This sets an upper limit to the value of the time-constant, RC , where R is the equivalent resistance of the transmitter, and C is the capacity of the trays and interconnector cables. The value of R has been made low by using two triodes (pentodes connected as triodes) in parallel, with the load in the cathode circuit. To lower it further would require more tubes and appreciably more power. It is therefore necessary to design the trays and connecting cords so that the maximum C to be driven is never larger than 5,000 micromicrofarads. Capacities from one line to another must be kept to a small fraction of the capacity to ground, in order to avoid cross-talk effects.

The flexible shielded cable which is available for use in making interconnection cables has a capacity of about 30 micromicrofarads per foot. If each cable is three feet long, and 30 such cables are used on a given trunk line, the capacity thus added may be of the order of 3500 mmfd. This leaves no more than 1500 mmfd. capacity for the trays and their short interconnection cables or jumpers. If eight trays are used, a tray and its jumper must have a capacity less than 200 mmfd. Since an eight foot length of shielded cable would have more than this, it is not possible to use this for running digit trunks and program lines the length of the ENIAC. Special coaxial lines would not only be expensive, but would excessively complicate the job of connecting in the sockets which are to occur every two feet.

The tray design which has been adopted is nearly equivalent to a coaxial line with convenient openings every two feet. The shielding is not perfect, but cross-talk is reduced to less than five per cent for even the worst combination of conditions. The maximum cross-talk then amounts to a two-volt pulse, which can have no effect since it is applied to the grids of input tubes biased at -20 volts, with cut-off at -8 volts.

Clearly, there cannot be too many jumpers connected to a particular digit trunk or program line or else the capacity given above would be exceeded. To assist the operator in determining the maximum safe loading the following term is introduced.

One load unit is a capacity of 160 micromicrofarads. The following devices will each be called one load unit:

(1) A program or digit cable. If the cable is only three feet long, it will account for about 90 mmfd. The balance is allowed for the portion of the circuits which will be internal at the particular panel to which the cable is connected.

(2) A tray and its short jumper for connecting to the next tray. The tray accounts for about 120 mmfd, and the balance easily accounts for the jumper.

The standard transmitters used on the regular program and digit outputs (not certain multiplier and divider outputs) are designed to transmit into a line containing not more than 60 load units. Actually program transmitters can transmit into as many as 120 load units with the usual 2:1 safety factor.

11.2 DELETTERS

A deleter is usually used to delete non-significant figures, and is therefore used on the add or subtract output digit terminals. Various types of deleters and the connections made in each are illustrated on drawing PK-4-109. A deleter merely open-circuits the lines corresponding to unwanted digits. Note that when a deleter is used on the output of an accumulator the significant figure switch should be set to the number of figures not deleted. In this case, the subtract pulse will be sent out over the line belonging to the significant figure furthest to the right, next to the deleted digits. Thus, the subtract pulse is not deleted.

11.3 SHIFTERS

A shifter is used to shift the digit lines to either the right or the left, and is placed on the input terminals of an accumulator. Thus, a shifter is generally used to multiply by powers of 10. The reason for this is the difference in shape of the CPP as compared to the 10P.

An example of a +2 and a -2 shifter are given on PX-4-104A.

A + shifter. A + shifter multiplies by positive integral powers of ten. In the case of a +2 shifter (PX-4-104A) any pulses arriving over the units channel (terminal 1 of the socket "S") goes to terminal 3 (hundreds) of the plug (P). The plug is inserted in the input digit terminal of the accumulator. Note that terminals 9 and 10 of the socket are not connected and that terminals 1 and 2 of the plug are connected to ground. This grounding prevents the grids of the corresponding input gates from picking up any cross-talk or other noise.

A - shifter. The - shifter multiplies by negative integral powers of ten. In this case, the unused terminals of the socket (see PX-4-104A) are not connected but the unused channels of the plug "P" must be fed with nine pulses in case of a negative number in order to give the proper complement. Thus, if M99430 is multiplied by one tenth the result is M999430. Thus, the FM line (terminal 11 on S) must be connected to terminals 9, 10, and 11, on P in the case of a -2 shifter. An adapter of this type must be used on the input to an accumulator since otherwise the FM transmitter would have to drive three different digit lines instead of just one digit line and three grids of the input gates to the accumulator.

11.4 PULSE AMPLIFIER UNIT

A pulse amplifier unit consists of eleven standard transmitters which interconnect to trunks. Since the buffer unit transmits in only one direction, two units would be needed to completely interconnect two trunks. In counting the load units on a particular digit trunk, for example, the input to the buffer unit counts as only one load unit and

since the buffer unit contains its own transmitters none of the load units of the trunk transmitted into count as being on the first trunk. Thus, these buffer units allow the operator to practically double the number of units which may be connected together via a digit trunk system.

The buffer units are designed to sit on top of a group of programmer or digit trays. The units contain their own transformers for supplying the heater voltages. The d-c power and the a-c power for the heaters is furnished by sockets located near the floor between accumulators nine and ten and between accumulators fourteen and fifteen.

A block diagram of a buffer unit is given on drawing PX-4-301.

11.5 STATIC OUTPUTS

Each decade and PM unit of every accumulator has a static output socket, accessible from the back. To avoid capacity loads on the counter circuits, a large resistance is placed in series with each static output line. The time constant thus introduced into the static output circuits is large enough so that one addition time must be allowed for the operation of other circuits from these outputs. However, because the system is a static one, there is no cross-talk problem, and unshielded wires can be used for the static cables.

Static cables are used to interconnect units in the following cases:

- (1) To connect the multiplier and multiplicand accumulators to the multiplier, see PX-6-301.
- (2) To connect certain accumulators and perhaps certain decades of the master programmer to the printer, see PX-12-304.

(3) To connect the PL unit of the numerator and denominator accumulators to the divider, see PL-10-303.

PL-4-111 shows the wiring connections of a static cable.

11.6 SPECIAL DEVICES

11.6.1 Special Program Jumpers

As well as the regular program jumpers described in Section 11.1.2, there are loaded program jumpers and X-program jumpers.

A loaded program jumper is to be used when connecting one program output directly to another program input. The jumper is physically characterized by having an extra long plug at one end which contains the built-in load resistor. Such a jumper must never be used in connection with a program line which enters a tray system which has its own load box.

An X-program jumper is a jumper with three plugs attached. It is used to connect two nearby program terminals (input or output) to the same program line. It has no built-in resistor so one connection must go to a program tray system which has a load box.

11.6.2 Accumulator Interconnection Cables

There are special interconnection cables and load boxes for use with accumulators which determine whether they act as ten digit accumulators or whether two accumulators act as a twenty digit accumulator. For a description of these cables, see PL-5-391.

11.6.3 Multiplier Interconnection Cables

The multiplier interconnection cables fall into two classifications. First, those that connect the multiplier to its associated

accumulators, and secondly, those that interconnect the three multiplier panels. In the latter classification, damage to circuit elements and short circuits across the power supply may be caused by erroneously plugging a cable into the wrong socket. This possibility is avoided by removing prongs from plugs, and filling corresponding socket holes (where not used) in such patterns that erroneous connections are impossible.

Reference should be made to the following diagrams:

Interconnection of High-Speed Multiplier with Associated Accumulators	PX-6-311
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Static Output Cable	PX-4-111
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Accumulator Interconnector Cable (Mult.)	PX-5-131
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Cross reference should be made to the Operator's Manual,

PX-6-304.

11.6.4 Divider Interconnection Cables and Adapters

Since the divider and square rooter serves largely to program its associated accumulators, those interconnections which must be established between the two units mentioned for the purpose of communicating program instructions are made through cables as illustrated on PX-10-307, which drawing makes further reference to special cables and adapters used.

Cross reference should be made to the Operator's Manual,

PX-10-307.

11.6.5 Function Table Adapters

In order to disconnect the 9P gates (B' and L'4) from the synchronizing trunk line carrying the 9P, and to connect these gates to

the line carrying the CPP in the same trunk, an adaptor (PX-4-119) is used. This adaptor is connected where the synchronizing pulse trunk plugs into the back of panel No. 2 of the function table.

11.6.6 Other Adaptors

The remaining adaptors may be classified as; 1) special digit adaptors, 2) digit-program adaptors, and 3) printer adaptors.

The first group consists of adaptors which combine shifting and deleting characteristics and are shown on PX-4-117.

The second group serves to make possible the use of digit trays as program trays. Each adaptor (there are 50) consists of a box with a 12-prong digit plug at one end, connected to a mounted group of 11, two-opening program sockets at the other. These correspond to the 12-prong sockets in the digit trays, and the two-prong plugs on program cables.

The third group consists of two adaptors. Adaptor A (PX-12-114) connects the static output of stage M (of the printer interconnection cable to accumulator or master programmer decade counter stages) to the PM lead in each of two static output cables. Adaptor B is used when no connection is desired to the PM lead in the static output cables. Adaptor B is also shown on PX-12-114.







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